Y011208

STUDY OF CVD SILICON NITRIDE FOR MNOS DEVICES

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MS/2002/M
Su34s

MATERIALS SCIENCE PROGRAMME

Indian Institute of Technology Kanpur

MARCH, 2002

A139554

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A Thesis Submitted
in Partial Fulfillment of the Requirements
for the Degree of

Master of Technology

By

PRAVEENKUMAR SUGGISETTI

to the

MATERIALS SCIENCE PROGRAMME
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
MARCH 2002

29 APR 2002

/MME

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भारतीय प्रौद्योगिकी संस्थान कानपुर
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CERTIFICATE

It is certified that the work contained in the thesis titled "STUDY OF CVD SILICON NITRIDE FOR MNOS DEVICES", by PRAVEENKUMAR SUGGISETTI (Y011208), has been carried out under my supervision and this work has not been submitted for a degree.

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ABSTRACT

Chemical Vapor Deposited (CVD) Silicon Nitride films are extensively used in both Silicon and Gallium Arsenide device technology for applications such as, local oxidation of silicon (LOCOS), passivation of silicon devices, MNOS devices and a capping layer to prevent outdiffusion of arsenic from gallium arsenide. An atmospheric pressure chemical vapor deposition (APCVD) reactor was assembled for the deposition of silicon nitride using dichlorosilane and ammonia. Silicon nitride layers were deposited in the temperature range 750 –900 °C under various gas flow conditions. Deposition process and the layers were evaluated for deposition rate, etch rate, composition, dielectric constant, refractive index etc. Techniques, such as, RBS, IR, Interference and C-V have been used for characterization. MNOS capacitors were fabricated on both n-type and p-type silicon. Adherent, uniform silicon nitride films deposited in the temperature range 750-850 °C for high ammonia to dichlorosilane flow rate ratios. The measured dielectric constant, refractive index of the deposited films were compared with the standard values, and were matched. From the IR spectrum results it was observed that as deposition temperature increase the Si-N bond strength increases. The charge trapping at oxide-nitride interface has been observed and its effect on C-V plots evaluated. MNOS transistors were also attempted but transistor action was not obtained.

ACKNOWLEDGEMNTS

I wish to thank my thesis supervisor, Dr. Y.N.Mohapatra, for his guidance, suggestions and helps throughout the course of the thesis work. And I am extremely grateful to Dr.J.Narain for allowing me to work in his lab, and guiding me. He helped me, immensely and without his help and precious advises at all times, this project would never have been a success. He always there to help me and even at times went out of his way to lend an extra hand in the project. He patiently answered to all my queries. He stood by me even at late hours of night to complete the project. His close involvement and interest in this work motivated me highly to achieve the best.

I would also thank to Dr.R.S.Anand for giving me invaluable advises and suggestions. He was always there to help me and also gave time out of his busy schedule during the experiments. The encouragement and appreciation that he gave during the thesis work were very helpful. Without his help I wouldn't complete the thesis intime. I would like to thank Dr.Jitendra Kumar, Dr.K.Nrai and Dr.K.K.Kar for their suggestions.

I would like to thank Asha Ji, Giridhari, Sandesh, V.Laxman, Rama Rao, Malli, D.K.Sonkar, Ruchi, Bala, Mehrotra, Pavan, Venkat Reddy, Phani, R.Phani, Jeevan, Jitendra, Bhutani, Laxman, Nagendra, Sunder Raju, Narasimha and all of my classmates and juniors.

Finally I wish to convey my gratitude to my parents, sister and family for being the continuos source of support and inspiration to me.

To

My Parents

&

Chandra Sekhar

CONTENTS

Abstract **v**

Contents **vi**

List of Tables **ix**

List of Figures **x**

Chapter 1: 1 Introduction **1**

1.1 Objectives and Organization of the Thesis 1

1.2 Properties of CVD Silicon Nitride 2

1.3 MNOS Devices (Transistors & Capacitors) 3

1.3.1 Characteristics 4

Chapter 2: 2 CVD Process & Experimental Arrangement **9**

2.1 Types of CVD 9

2.2 Chemistry of CVD Reaction 9

2.3 Atmospheric Pressure Chemical Vapor Deposition (APCVD) of Silicon Nitride 10

2.3.1 Experimental Setup for Thermal APCVD 11

Chapter 3: 3. Characterization of Silicon Nitride **13**

3.1 Rutherford Backscattering (RBS) Measurement 13

3.2 Infrared Spectroscopy (IR) Measurement 19

3.3 Optical Interference Measurement 21

3 3 1 Preparation of Silicon Nitride sample for Refractive index measurement 21

3 4 Capacitance Voltage (CV) Measurements 24

3 4 1 Qualitative Description of Ideal MNS Capacitor 25

3 4 1 1 Accumulation 25

3 4 1 2 Depletion 26

3 4 1.3 Inversion 27

3 4 2 CV plots of MNOS Capacitors 29

Chapter 4: 4 MNOS Device Fabrication **31**

4 1 Procedure for Preparation of Masks 31

4 1 1 Photolithographic Process 35

4 2 Raw Material 36

4 3 MNOS Capacitor Fabrication 37

4.4 Transistor Fabrication 38

Chapter 5: 5 Results and Discussions **41**

5.1 Silicon Nitride Deposition 41

5.2 RBS Measurements 53

5.3 IR Measurement 60

5 4 Interference Measurement 65

5 5 CV Measurement 66

5 6 Memory behavior of MNOS devices 67

Chapter 6: 6. Conclusions and Future scope of thesis **73**

References **74**

LIST OF TABLES

Table No.	Title	Page No.
5 1	Deposition characteristics of silicon Nitride at Various deposition conditions	42
5 2	Composition and simulated thickness obtained from RBS measurement and physical thickness obtained From the interferometer measurement	53

List of Figures

Figure No.	Caption	Page No.
1 3	Cross sectional structure of MNOS (a) Capacitor (b) Transistor	4
1.3 1	Schematic illustration of the state of the trapping Centers and the free carriers at the silicon surface for (a) Traps neutral, gate potential at ground; (b) Traps being charged, gate potential at +v; (c) Traps charged, gate potential at ground; (d) Traps being discharged, gate potential at –v	5
1 3 2	Energy – band diagrams showing the current transport, trapping, and detrapping of electrons (a) Programmed with a positive voltage. (b) Erasing with a negative gate voltage.	6
1.3.3	The drain current I_D characteristics (vs V_G for a fixed V_D) of a p-channel MNOS transistor, showing the change of threshold voltage after (a)erase and (b) program	7
2 3.1	Experimental arrangement made for deposition of silicon nitride	12
3 1.1	Schematic diagram of basic back scattering spectroscopy	14
3.1.2	Basic back scattering spectrometry (a) Experimental geometry	16

(b) Back scattering spectrum for the two-element compound (A_mB_n) film of uniform composition on a low mass Substrate
3 3 1 (a) Flow chart 23
(b) Top and side view of the prepared Silicon Nitride sample
3 4 CV measurement setup 24
3 4 1.1 Surface accumulation in MNS capacitor fabricated on p-type Silicon substrate 25
3 4 1 2 Surface depletion in MNS capacitor 26
3 4 1 3 Surface inversion in MNS capacitor 27
3 4 1 4 CV plots of MIS Capacitor fabricated on p-type substrate 28
3 4 1 5 CV Plots of MIS Capacitor fabricated on n-type substrate 29
3.4 2 CV plots of MNOS capacitor (n-type substrate)
3.4.3 CV plots of MNOS capacitor (p-type substrate) 30
4 1.1 Flow chart for Mask making 32
4.1.2 Mask 1 33
4 1.3 Mask 2 33
4.1.4 Mask 3 34
4.1.5 Mask 4 34
4.1.1.1 Flow chart for Photolithographic process 35
4.3.1 Process flow chart for fabrication of MNOS capacitor 37
4 6 (a) Flow chart for fabrication of MNOS transistor 40
(b) Top view of the transistor designed

5 1 1 Variation of deposition rate with temperature at constant dichlorosilane, ammonia and nitrogen flow rates 20ml/min, 500 ml/min and 1 lit/min respectively 44
5 1.2 Variation of deposition rate with increase of dichlorosilane for a fixed ammonia and nitrogen flow rates 500 ml/min and 1 lit/min respectively at temperatures (a)750 °C (b) 850 °C. 45
5 1 3 Variation of Silicon Nitride thickness with Ammonia to dichlorosilane ratio Series 1-25, series 2-20, series 3-17 (a)750 °C (b) 850 °C 46
5.1.4 Variation of Etch rate of the deposited silicon nitride films with Deposition Temperature 47
5 1.5 Variation of Etch Rate with Deposition Temperature after one hour annealing at 950 °C 48
5.1.6 Variation of Etch Rate with Deposition Temperature after one hour Annealing at (a) 1000 °C and (b)1050 °C 49
5.1.7 Silicon nitride film deposited at 750 °C 50
5.1.8 Silicon nitride film deposited at 800 °C 51
5.1.9 Silicon nitride film deposited at 850 °C 51
5.1.10 Silicon nitride film deposited at 900 °C 52
5 1.11 8000 A° film deposited at 900 °C 52
5.1.12 12000 A° film deposited at 850 °C 53
5.2.1 RBS and simulated spectra of Silicon nitride 54

deposited at 750 °C

5 2 2 RBS and simulated spectra of Silicon nitride 55
deposited at 800 °C

5 2 3 RBS and simulated spectra of Silicon nitride 56
deposited at 850 °C

5 2.4 RBS and simulated spectra of Silicon nitride 57
deposited at 900 °C

5.2.5 RBS and simulated spectra of Silicon nitride 58
deposited at 850 °C

5 2 6 Variation of Composition with, deposition temperature 59
(a) Silicon to Nitrogen ratio
(b) Silicon to oxygen ratio

5.3 1 IR Absorption Peak shift with Deposition Temperature 60

5 3.2 IR Absorption spectra of Silicon Nitride deposited at 750°C 61

5.3.3 IR Absorption spectra of Silicon Nitride deposited at 800°C 62

5.3 4 IR Absorption spectra of Silicon Nitride deposited at 850°C 63

5.3.5 IR Absorption spectra of Silicon Nitride deposited at 900°C 64

5.4.1 Variation of Refractive Index with Deposition Temperature 65

5.5.1 Variation of Dielectric Constant with Deposition Temperature 66

5.6.1 CV characteristics of n-type substrate MNOS capacitor, by application 67
of different negative gate voltages

5 6.2 CV characteristics of n-type substrate MNOS capacitor, by application 68
of different positive gate voltages

5 6 3 CV characteristics of p-type substrate MNOS capacitor, by application of different positive gate voltages 69

5 6 4 Magnified picture of n-channel MNOS transistor fabricated (20 A° wet oxide, 1400 A° silicon nitride) 70

5 6.5 Magnified picture of p-channel MNOS transistor fabricated (40 A° dry oxide, 1250 A° silicon nitride) 71

5 6 6 Magnified picture of p-channel MNOS transistor fabricated (60 A° dry oxide, 1250 A° silicon nitride) 71

5.6 9 Magnified picture of n-channel MNOS transistor fabricated (60 A° dry oxide, 1500 A° silicon nitride) 72

Chapter 1

1. Introduction

Chemically deposited silicon nitride films are extensively used in both silicon and gallium arsenide device technology for many device applications. Such as gate dielectric of MNOS silicon nonvolatile devices and capping material for Gallium Arsenide for high temperature annealing. A well-designed and fabricated MNOS memory device can have memory retention more than 100 years Some of the other device applications of silicon nitride are as a mask, and for passivation. It serves extremely good barrier to the diffusion of water and sodium because of its dense structure. These impurities cause device metalization to corrode or devices to become unstable. Since oxygen diffuses very slowly through nitride, deposited nitride can prevent oxidation of underlying silicon. This property is exploited in local-oxidation-of-silicon (LOCOS), which is essential for VLSI planar device technology Si_3N_4 is also an excellent diffusion mask for gallium, and is used for making junctions with this dopant in power device applications.

1.1 Objectives and Organization of the Thesis

Silicon nitride films are needed for many device applications especially for MNOS devices. Hence it has been the aim of this work to deposit silicon nitride films and fabricate MNOS devices (capacitors, transistors) So I have assembled a CVD reactor and optimized the silicon nitride deposition for MNOS device application. The deposited silicon nitride films have been characterized using the measurements employed by Rutherford Backscattering Spectroscopy (RBS), Infrared Spectroscopy (IR), Capacitance Voltage (CV), and Optical Interference. And MNOS devices have been fabricated on both p-type and n-type silicon wafers.

The thesis has been organized into six chapters. A brief introduction to silicon nitride and MNOS devices is discussed in the chapter 1. A general discussion about chemical vapor deposition (CVD) and experimental setup prepared in the lab is described in the chapter 2. An introduction to the characterization techniques used i.e. Rutherford Backscattering Spectroscopy (RBS), Infrared Spectroscopy (IR), Capacitance Voltage (CV), Optical Interference for the deposited nitride is described in chapter 3. It also provides the experimental arrangements for RBS and CV measurements. Chapter 4 deals with the experimental procedure used in this work for fabrication of MNOS devices. Chapter 5 details the experimental results of characterized silicon nitride and observed memory effect of the MNOS devices. Chapter 6 summarizes the study and suggests avenues for future.

1.2 Properties of CVD Silicon Nitride

Silicon nitride, in its stoichiometric form, has a composition given by Si_3N_4, but depending on deposition conditions and deposition method one can get Si/N ratios from 0.7 to 1 and dielectric constant 5.5-8, refractive index 1 8-2.05, density in between 2.3 to 2.8 g/cm^3.

Thermal silicon nitride, chemically deposited at atmospheric pressure and temperatures is an amorphous dielectric and contains hydrogen up to 8%. The Hydrogen is bonded to nitrogen and the silicon. The amount of hydrogen depends on the temperature and the ratio of the reactants. More hydrogen is incorporated at low deposition temperatures and or at high ammonia to dichlorosilane ratios. Silicon nitride deposited at low ammonia to dichlorosilane ratios contains excess silicon that decreases the electrical resistivity. Silicon nitride films have a refractive index of 2 and etch rate less than 50A°/min in buffered HF at room temperature. Silicon nitride has a high tensile stress, about $10^{10} dyne/cm^2$. Films thicker than 200*nm* sometimes crack because of high stress. The electrical resistivity depends on the deposition temperature, film stochiometry, amount of hydrogen in the film, and the presence of oxygen impurities [1-2].

As discussed above that silicon nitride is an excellent barrier to sodium diffusion. So its effectiveness is usually tested by evaporating radioactive sodium chloride on the silicon nitride and then heating the samples. The sodium that diffuses into the film is counted as the silicon nitride is removed by step etching [3]. The properties of pure silicon nitride are:

Dielectric strength	10^7 *V/cm*
Bulk resistivity	10^{16} Ohm-cm
Dielectric constant	5 5 – 8
Energy gap	5 eV
Thermal expansion	4 x 10^{-6} */°C*
Stress at 23°C on Si	1.2 –1.8 x 10^{10} *dyne/cm*^{2} (Tensile)
IR absorption (Si-N)$_{max}$	880 *cm*$^{-1}$
H_2O permeability	zero

1.3 MNOS Devices (Transistors & Capacitors)

MNOS(metal-nitride-oxide-semiconductor or metal-nitride-oxide-silicon) devices belong to a group of MIOS(metal-insulator-oxide-semiconductor) structures having a special feature of dual gate dielectrics-insulator on oxide [4-5]. With nitride being the most popular, other insulators include Alumina, tantalum oxide, and titanium oxide. The use of these MNOS devices are two fold, depending on the oxide thickness. If the oxide is very thin they can be used as memory devices otherwise they can be used as MOS devices. The advantage of MNOS devices over MOS devices is the nitride layer serves as a barrier for migrating ions, which prevents the threshold shift of MOS devices and in addition preserves the quality of oxide-silicon interface. In the present work our inters is in MNOS memory devices [5-8].

The structure of MNOS devices is similar to MOS devices except that the gate is dual dielectric. In the case of memory devices the oxide layer is in the range 20-80 A° thick and is thermally grown on silicon substrate. The purpose of this oxide film is to provide good interface to the semiconductor, and to prevent back tunneling of the injected charge for better charge retention. Typically, the deposited nitride layer ranges from 200 A° to 1200 A° thick. The thickness has to be balanced between programming voltage and charge retention: not so thick that it causes excessive programming voltage, and not so thin that the stored charge leaks to the gate. Both channel types have been used but p-channel devices are more common [8-12] The structure of MNOS capacitor and P-channel transistor is shown in Fig1.3.

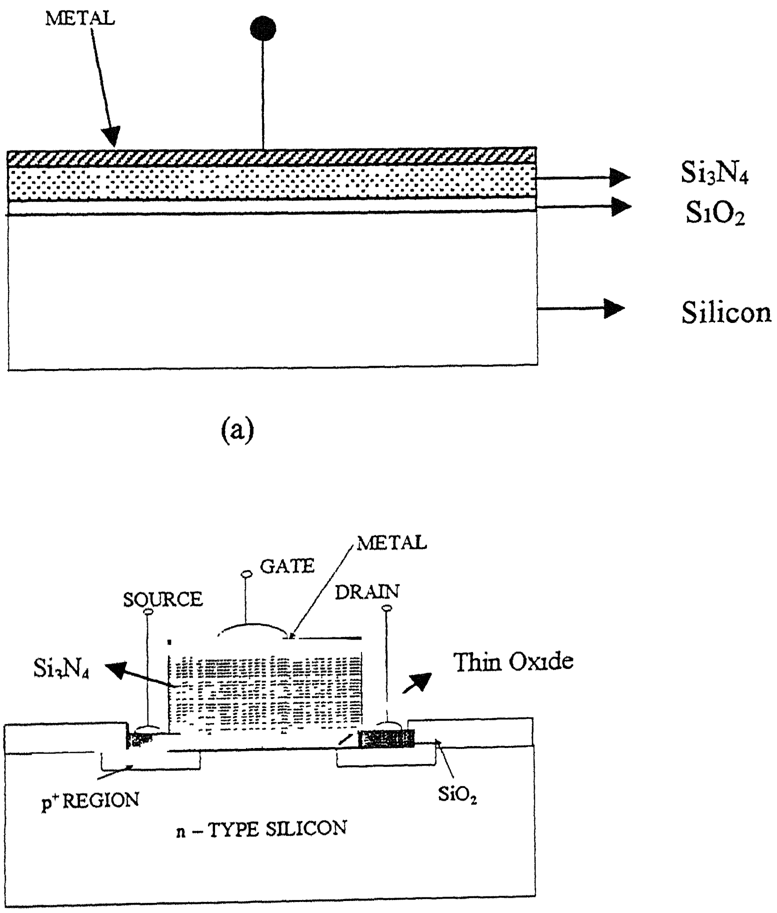


Fig.1.3. Cross sectional structure of MNOS (a) Capacitor (b) transistor

1.3.1 Characteristics

The MNOS devices operate on the principle of charge storage on traps at an interfac. On application of a positive gate voltage electrons from substrate tunnel the thin oxide and are trapped in the nitride layer near to the oxide-nitride interface, giving rise to a negative charge sheet (Q_n *in* C/cm^2) that is uniformly distributed above the channel.

The negative charge sheet changes the threshold voltage of the MNOS device This charging process is called programming. By sensing the threshold voltage, memory can be read The reverse process or discharge is called erase, which returns the threshold voltage to its original value. The charging and discharging of these devices is shown in Fig.1.3 1

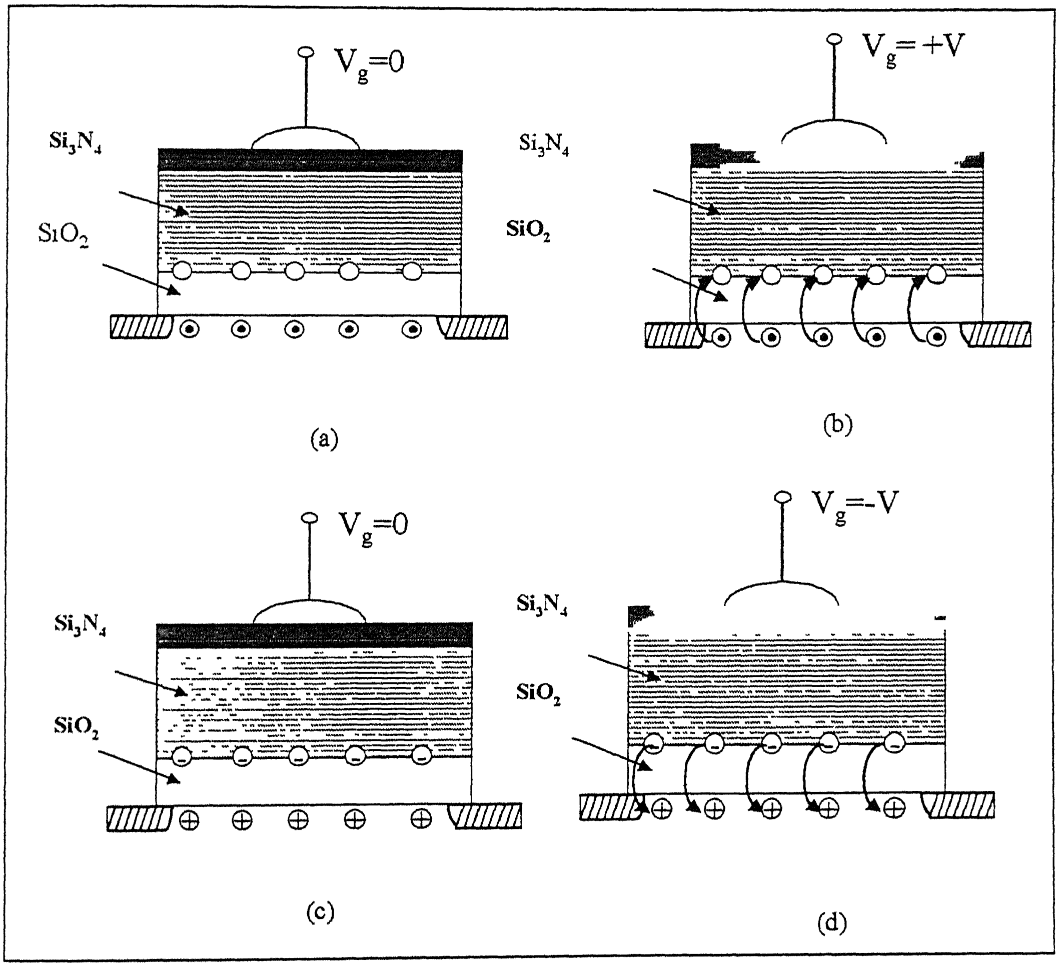


Fig.1.3.1. Schematic illustration of the state of the trapping centers and the free carriers at the silicon surface for (a) traps neutral, gate potential at ground; (b) traps being charged, gate potential at +V, (c) traps charged, gate potential at ground; (d) traps being discharged, gate potential at -V

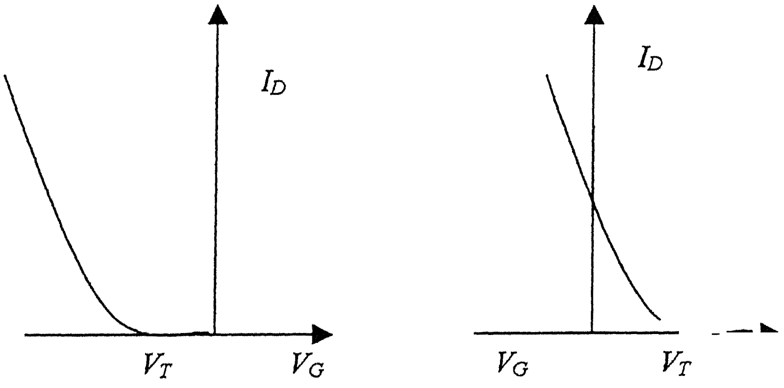
The thresh hold voltage for a p-channel device is given by

$$V_T = V_{FB} - 2\psi_B - \frac{\sqrt{4\varepsilon_s q N_D \psi_B}}{C_G} - \frac{Q_n}{C_n} \tag{1.3.1}$$

The total gate capacitance C_G is equal to the serial combination of the nitride capacitance C_n and oxide capacitance C_{ox}, given by

$$C_G = \frac{1}{(1/C_n)+(1/C_{ox})} = \frac{C_{ox}C_n}{C_{ox}+C_n} \tag{1.3.2}$$

Where ε_n and ε_{ox} are the permitivities of nitride and oxide, respectively. After programming, the negative charge sheet increases the threshold voltage (less negative), often to a positive value so that the transistor becomes a depletion mode device (normally-on). The drain current characteristics after programming and erase are shown in the following Fig.1.3.3



(a) (b)

Fig.1.3.3. The drain current I_D characteristics (vs. V_G for a fixed V_D) of a p-channel MNOS transistor, showing the change of threshold voltage after (a) erase and (b) program.

In the programming process, a large positive bias is applied to the gate. Current conduction is known to be due to electrons, which are emitted from the substrate to gate as shown in fig. The conduction mechanisms in the two dielectric layers are very different, and have to be considered in series. The current through the J_{ox} is by tunneling

Notice that electrons tunnel through the trapezoidal oxide barrier, followed by a triangular barrier in the nitride [13,14]. This form of tunneling has been identified as modified Fowler-Northeim tunneling through a single triangular barrier, which has the following form

$$J_{ox} = C_1 E_{ox}^2 \exp\left(-\frac{C_2}{E_{ox}}\right) \qquad (1.3.3)$$

Where E_{ox} is the filed in the oxide layer. The theory for modified Fowler-Nordheim tunneling is much more complicated. The current through the nitride layer J_n is controlled by Frenkel-Poole transport, which has the following form

$$J_n = C_3 \varepsilon_n \exp\left(\frac{-\phi_B + \sqrt{qE_n/\pi\varepsilon_n}}{\phi_T}\right) \qquad (1.3.4)$$

Where E_n is the electric field in the nitride, ϕ_B is the trap level below the conduction band (≅ 1 3 eV) and $C_3 = 3 \times 10^{-9}\ (\Omega\text{-}cm)^{-1}$. The charging process of the traps is governed by

$$-\frac{dQ_n}{dt} = J_{ox} - J_n \qquad (1.3.5)$$

$$\varepsilon_{ox} E_{ox} = \varepsilon_n E_n + Q_n \qquad (1.3.6)$$

$$x_{ox} E_{ox} + x_n E_n = V_p \qquad (1\ 3.7)$$

Where V_p is the programming gate voltage It is known that at the beginning of the programming process, the modified fowler-Nordheim tunneling is capable of a higher current and conduction is limited by Frenkel-Poole transport through the nitride layer. When the negative charge starts to build up, the oxide field decreases and the modified Fowler-Nordheim tunneling starts to limit the current. The programming speed is largely affected by the choice of the oxide thickness, and a thinner oxide allows a shorter programming time. Programming speed has to be balanced with charge retention since too thin an oxide will allow the trapped charge to tunnel back to the silicon substrate. Typical threshold shift is 5-10 V, with a programming gate voltage between 15V and 30V. The high programming voltage is a disadvantage [15-19]

Chapter 2

2. CVD Process & Experimental Arrangement

Chemical vapor deposition (CVD) is a process where one or more gaseous species react on a solid surface and one of the reaction products is a solid phase material In the process, gaseous compounds of the materials to be deposited are transported to the substrate surface and decomposition, deposition takes place.

The advantage of the CVD process is, most of the reactants used are gases, thereby taking advantages of many characteristics of gases. Through CVD process one can deposit metals, semiconductors, insulators and can get desired properties by adding dopants or by changing the process variables such as temperature, pressure and flow rates of the reactants. One can get high purity nearly 99.99% and nearly 100% theoretical density films [20].

2.1. Types of CVD

For deposition to take place one has to decompose the reactants by supplying activation energy. This activation energy can be supplied by thermal or plasma or acoustic or photon by some other means. Depending on the way which the energy supplied to decompose the reactants, the process is called Thermal CVD or Plasma enhanced CVD or acoustic CVD or photo CVD and so on. Each process has its own merits and demerits. One uses the different CVD process depending on the application. And also depending on pressure i.e., low pressure of atomospheric pressures its called low-pressure chemical vapor deposition (LPCVD) or atmospheric pressure chemical vapor deposition (APCVD).

2.2 Chemistry of CVD reaction

When gaseous compounds of the material to be deposited are transported to the substrate where reaction or deposition occurs.

Important steps are,

1. Mass transport in the bulk gas flow from reactor inlet to deposition chamber.
2. Gas phase reaction.
3. Mass transport of film reactants to growth surface.
4. Adsorption of film reactants on growth surface.
5. Surface diffusion of film reactants
6. Incorporation of film constituents into growing film.
7. Desorption of byproducts.
8. Mass transport of byproducts to the exhaust.

In all CVD process, dealing with the change from one state i.e., the initial, low temperature reactant gases to, later i.e., the final state with some solid phase and product gases in time. The deposition rate depends on chemical kinetics and fluid dynamic transport phenomena and surface conditions such as temperature. The CVD process will tend to be limited by the rate at which reactants can get to the surface or products leave it. The deposition rate decreases with decreasing pressure At low pressure, the mean free path and diffusivity increases by several orders of magnitude. It allows an significant increase in the rate of transfer of reactant gases to, and by-products from the substrate surface.

2.3. Atmospheric Pressure Chemical Vapor Deposition (APCVD) of Silicon nitride

As discussed above that the CVD reaction, which takes place at atmospheric presuure, is called APCVD. APCVD reaction rate controlled by reaction temperature, reactant concentrations, and temperature gradients in the furnace [21]. And the experimental arrangement for APCVD is relatively simple compared to others.

At atmospheric pressure silicon nitride can be chemically deposited by reacting dichlorosilane and ammonia or by reacting silane and ammonia in the temperature range 700 ^{o}C and 900 ^{o}C.

The chemical reactions are,

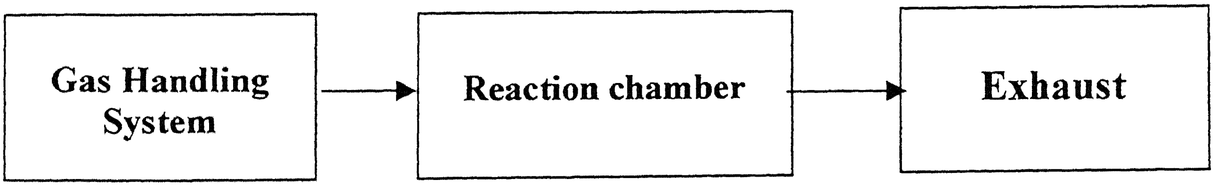
$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$$

$$3SiH_4 + 4NH_3 \rightarrow SiN_4 + 12H_2$$

2.3.1 Experimental setup for thermal APCVD

A typical CVD apparatus consists of the following basic requirements.

- Gas handling system
- The Reactor
- Exhaust system



Silicon nitride CVD system is significantly different from other systems because of the nature of the gases that are used [22]. The system is setup according to the description given by William A. Brown et al [23]. I used dichlorosilane and ammonia for silicon nitride deposition. These gases are highly reactive with each other at room temperature and therefore had to be separately fed into the reactor. I also used nitrogen as a carrier gas and therefore I had to install three separate lines form different gas cylinders to the reactor. The line from the nitrogen system to the reactor was of nylon tubing with inner diameter 6 mm. The lines from the ammonia cylinder and dichlorosilane cylinder to the reactor were made of stainless steel. The reactor was made up of quartz of inner diameter 55 mm and lengh120 cm. The gases were fed from the quartz tube of inner diameter 5 mm and outer diameter 7 mm through a brass adapter.

The furnace is made of Kanthal wire wound on a ceramic tube, with the wire resistance being 17 Ω The gases are passed through the flow meters and then passed to the reactor quartz tubes by Teflon tubes. The brass adapter is tightened to the quartz tube by rubber piece with the help of vacuum grease A fan arrangement also made at this point to cool the brass adapter Wilson seal arrangement is made to the tubes, where gases fed to the reactor at the brass adaptor. Teflon tape is used at the joints and other places to avoid the leakage of the gases. The experimental arrangement made is shown in Fig. 2 3.1 Another separate nitrogen line is connected to the dichlorosilane line for purging the line before and after passing the dichlorosilane. To avoid blockage in dichlorosilane line, the dichlorosilane is diluted with nitrogen by connecting another nitrogen line to it.

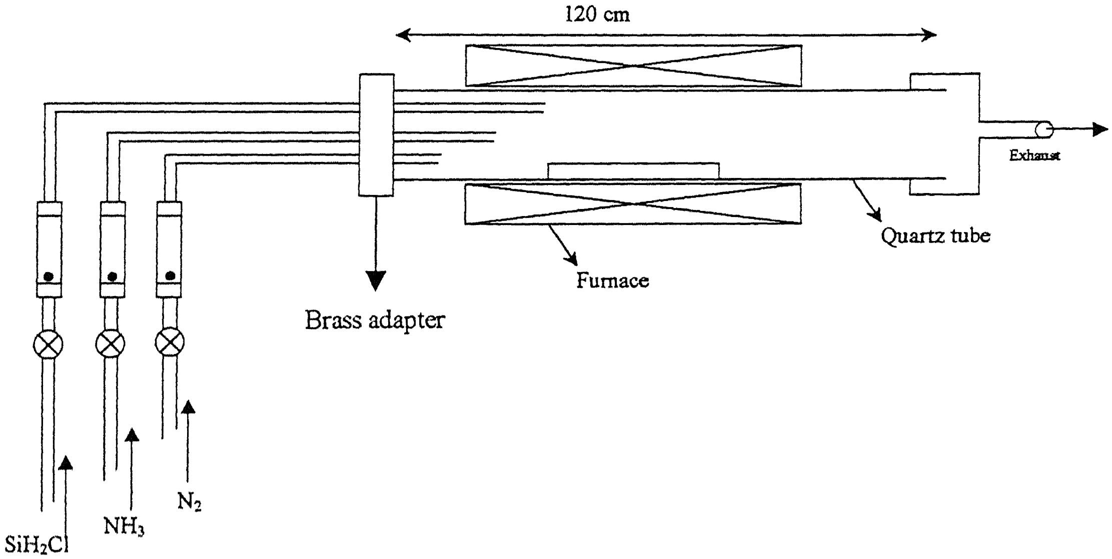


Fig. 2.3.1 Experimental arrangement made for deposition of silicon nitride

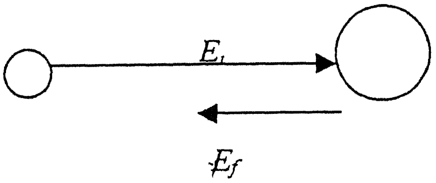
Chapter 3

3. Characterization of Silicon Nitride

To characterize the deposited silicon nitride films, Rutherford Backscattering Spectroscopy (RBS), Infrared Spectroscopy (IR), Capacitance Voltage (CV), Conductance and Optical Interference measurements were employed. A general introduction to these characterization techniques is presented in this chapter. It also depicts the experimental arrangements for RBS, IR, and CV.

3.1. Rutherford Backscattering (RBS) Measurement

RBS (Rutherford backscattering) is a surface analysis technique, which gives quantitative information on elemental composition and depth profiling without the use of standards This technique has been used to find stochiometry of the deposited films. The physical concept behind RBS is quite straightforward[16]. When energetic ion recoils from an elastic collision with an atom (no angular deflection), its energy depends on the mass of the atom it hit. Such a collision is schematically in figure. Typically a doubly-ionized helium ion is used in the probe beam.



The backscattered energy is simply

$$E_f = E_i \left(\frac{M-m}{M+m}\right) \tag{3.1.1}$$

When using the He^{++} ion accelerated to 2 *MeV*, the RBS procedure is most sensitive to the heavier atoms. And also the probability of a scattering collision occurring is larger for heavier atoms. So the number of counts detected, for the same dose is substantially higher for heavier atoms [17].

A second feature of RBS is its ability to give concentration versus depth. As the He^{++} ion traverses the sample, it loses energy because it undergoes many grazing collisions before it hits an atom head-on and recoils. Similarly, on its way back through the sample, it again loses energy. This energy loss can be used to evaluate the depth at which the collision occurred. A typical back scattering system is shown in the following Fig 3 1 1

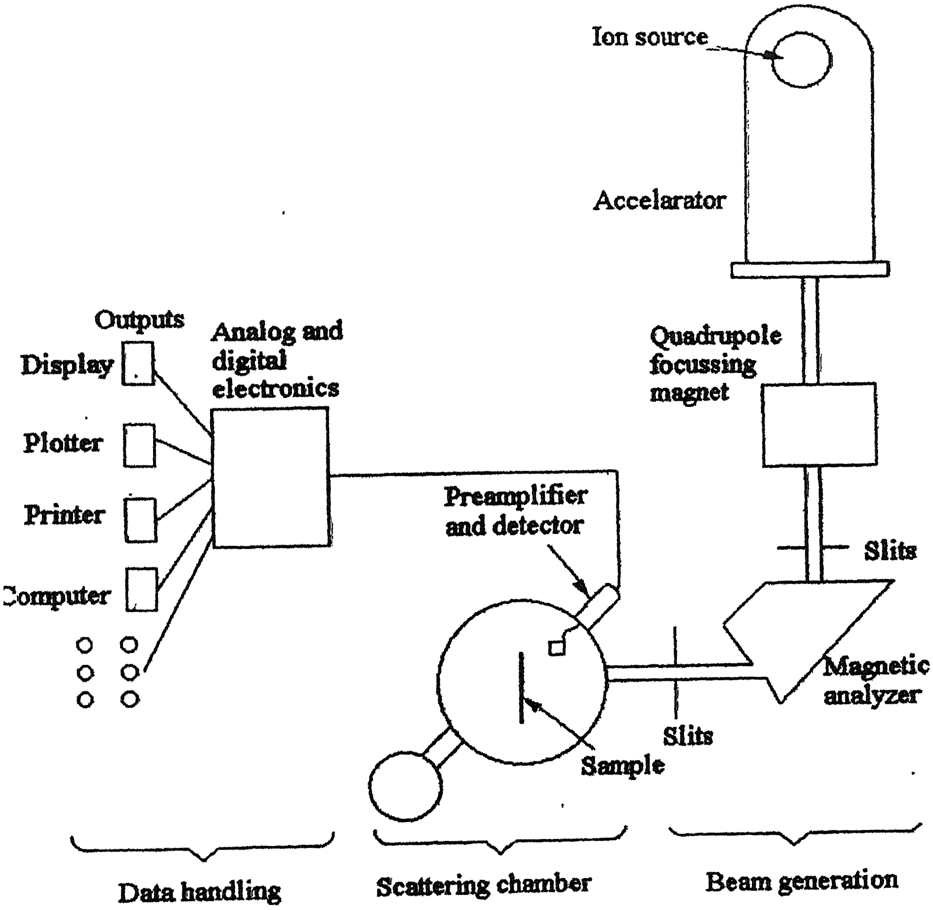


Fig. 3.1.1. Schematic diagram of basic back scattering spectroscopy

A beam of monoenergitic and collimated ions (preferably $^4He^{++}$) having several MeV (obtained from a Van-de-Graff or similar accelerator) impinges perpendicularly on the surface. Analysis ions scatter elastically from target atoms with energy characteristic of the mass of the struck particle and lose energy passing into and out of the film material. The ions scattered backward at an angle of more than 90° (usually in the range 120 °-170°) with respect to the incident direction, can be collected to produce an electrical signal by employing a suitable detecting system. The output of this system is an analog signal, which is processed by a multichannel analyzer. The multichannel analyzer subdivides its magnitude into a series of equal increments. Each increment is numbered and referred to as a channel. There are thousands of channels in a modern multi channel analyzer. An event whose magnitude lies within a particular channel is registered there as a count. The signal, after processing with associated electronics, displays a spectrum in the form of counts per channel vs. channel number, yielding information about the depth distribution profile of atomic concentrations in the sample under test. In the graphical display count per channel is generally normalized with respect to a particular count and is labeled as normalized yield. The channel number is normally linearly related to the backscattered ion energy and the relation between them is a characteristic of the system and can be determined experimentally. Appearing in the spectrum is nearly flat-topped "peak" for each element in the film. The peak widths are caused by the energy loss of the helium ions in the film material. If the energy of the incident ions is high, collision with the nuclei can be considered to be elastic in nature resembling collision of two hard spheres.

Fig.3.1.2 show the experimental geometry and observed back scattering spectra of a two-element compound. The film elements may identified by insertion of measured energies (E_1^A, E_2^B) of the high-energy sides from the peaks of the measured RBS spectra Fig. 3.1.2 into

$$K_i = E_1^{1} / E_0 \qquad (3.1.2)$$

To calculate the kinemetic factor K for the ith element. E_o is the incident ion laboratory kinetic energy. Gold, having atomic mass of 197 amu (atomic mass unit) has K factor 0.9225 at an angle of 170°. thus for 1 MeV He^{++} ions the backscattered particles will have energy of 0.9225 MeV. The kinematic factor K is given by,

$$K = \left[\frac{\left(M_2^2 - M_1^2 \sin^2 \Theta\right)^{1/2} + M_1 \cos\Theta}{M_1 + M_2} \right]^2 \qquad (3\ 1.3)$$

where θ is the laboratory angle through which the incident ion is scattered, and M_1, M_2 are the masses of the incident and target particles, respectively. As the parameters M_1, E_o and θ are usually known, M_2 us determined and the target element is identified.

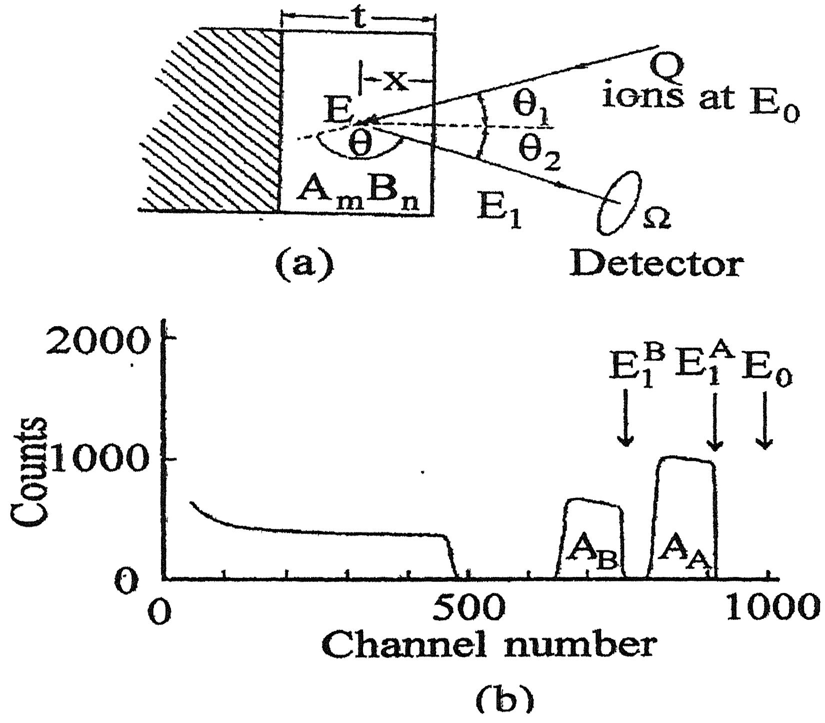


Fig. 3.1.2. Basic back scattering spectrometry. (a) Experimental geometry, (b) Back scattering spectrum for the two-element compound (A_mB_n) film of uniform composition on a low mass substrate.

The areal density, $(Nt)_i$ in atoms per unit area, may be determined for the ith element from knowledge of the detector solid angle, Ω, the integrated peak count A_i for Q incident ions, and the measured or calculated cross section $\sigma_i(E, \theta)$ using

$$(Nt)_i = \frac{A_i \cos\Theta_i}{2\Omega\sigma_i(E,\Theta)} \qquad (3.1.4)$$

Here, N_i is the atomic density (atoms per unit volume) of the ith element and t is the physical thickness.

The average stoichiometric ratio for the compound film (A_mBn) may be calculated from equation 3.4 to be

$$\frac{n}{m}=\frac{N_B}{N_A}=\frac{A_B\sigma_B(E,\Theta)}{A_A\sigma_A(E,\Theta)} \tag{3 1 5}$$

It can be noted that this ratio depends only on the ratio of measured integrated peak counts A_A/A_B and knowledge of the cross-section ratio σ_A/σ_B, the hard-to measure quantities Q and Ω have cancelled.

A probing He atom loses finite amounts of energy during encounters with atoms in a simple. As a result, the spacing (density) of atoms will have a direct effect on the amount of energy lost by a probe atom versus the distance (depth) it traverses. Knowledge of film density, ρ_{AB} is required to convert areal densities, $(Nt)_I$ to physical film thickness, to the relevant atomic densities, N_A^{AB} and N_B^{AB}, may be calculated from

$$N_A^{AB}=\frac{m\rho_B N_0}{M_{AB}} \qquad N_B^{AB}=\frac{m\rho_A N_0}{M_{AB}} \tag{3.1 6}$$

And then used in to calculate thickness (t),

$$t=\frac{(Nt)_A}{N_A^{AB}}=\frac{(Nt)_B}{N_B^{AB}} \tag{3.1 7}$$

Here N_o is the Avogadro's number and $M_{AB} = mN_A + nM_B$ is the molecular weight of compound A_mB_n.

An RBS rectangular profile of the massive element (mass M_A) appears as a rectangular signal in the spectrum at higher energies. Also, the profile of light element (mass M_B) produces a signal at lower energies. It anticipates that heavy and light masses create signals at high and low energies respectively Nevertheless, their yields have different levels through atomic concentrations of these species in the alloy are equal If the atomic number is more, the yield is high and, if the atomic number is less, the yield is low. Therefore it can be concluded that yield increases with the atomic number. Thus, in the backscattering spectrum, each element has its own coordinate system deranged on the abscissa. The discussion so far is qualitative. In quantitative facto *K* determines the place on the X – axis of the backscattered spectrum where the signal of an element has its high energy or "leading" edge.

The locations of the edges are also labeled at energies $E_1^A = K_A E_O$ and $E_1^B = K_B E_O$, Where K_A and K_B are the kinematic factors of the elements A and B respectively. Analogously, the scattering cross section σ gives the scaling factor for the yield axis of different elements. The relative concentration ratio of the two elements transfers into relative yields by ratio given essentially by their relative scattering cross section or $(Z/z)^2$. The energy span in the spectrum represents thickness of the film but interval (or scale) for each mass is not the same. This interval differs by about 10% or less and on that account correction is essential.

Another approach to analyzing backscattering spectra is by computer simulation involving the calculation of the energy spectrum of backscattered particles using a specified target composition and experimental parameters. It is performed by altering the target composition until the calculated and measured energy spectra are closely matched. It can be done either by manually changing the target composition e.g. film thickness or areal density, relative amount of the individual elements of the sample, for each iteration or by using a least-square fitting procedure to find the target composition that best fits the measured spectrum. A well-known backscattering analysis program, RUMP which originated at Cornell University has been used here.

Finally, we must note that RBS gives no information on chemical bonding, so it may be necessary to use another technique to establish the nature of any compound being studied. Nonetheless, the RBS is unique in that it can provide quantitative elemental composition data.

3.2 Infrared Spectroscopy (IR) Measurement

Infrared spectroscopy (IR) is a technique used to determine the chemical nature of a thin film. It gives the quantitative information of the film, which is not provided by RBS spectra Some materials will absorb certain frequencies in the infrared (wavelength 2 to 25 microns) because of the excitation of vibrational energy transitions in molecular species The vibration of molecule (stretching or bending) will have a resonance value, and it will be excited by radiation of this frequency. When infrared radiation of a particular frequency is passed through a sample containing molecular species, it may or may not be absorbed. If all frequencies are passed through, some will be absorbed to varying degrees, depending on the molecular species involved. So one can notice absorption peak at that particular frequency. For complex molecules with many vibrational modes, there are many absorption peak frequencies

There are two types of spectrometers that one can use to generate such spectra. One uses a monochromator to evaluate each frequency in turn. The second uses a Michelson interferometer to examine all frequencies simultaneously, and then a Fourier transform to display the spectrum. The advantage of the latter approach is its greater sensitivity, and the speed with which it can produce a spectrum.

Regardless of how it is obtained, the spectrum can be used to make quantitative estimates of the concentration of molecular species in thin films. Using the Beer-Lambert Law, we can write simply,

$$A = ECL \qquad (3.2.1)$$

Where

A = absorbance = $log_{10} I_0/I$

I_0 = incident radiation

I = transmitted radiation

E = extinction coefficient

L = path length

C = concentration

Absorbance can be obtained from the spectra. Path length is nothing but thickness of the film and the extinction coefficient is a characteristic of a substance. Then measurement of A and L gives a resulting value for C.

Infrared radiation comes from the IR sources and passes through the sample, and detector detects this IR radiation. When ever the frequency of vibration matches the IR frequency then sample absorbs the radiation and dip in IR absorption spectra can be noticed at that frequency.

3.3. Optical Interference Measurement

The refractive index and thickness of thin films can be determined by optical interference technique. The knowledge of this index of refraction can be used to infer the chemical composition. Depending on the deposition conditions of the films, their stoichiometry can be varied. It turns out that this variation in stoichiometry can be related to the measured refractive index. Accordingly, measurements of the refractive index can be used as an approximate guide to film stoichiometry

For measurement of index of refraction of the deposited films, a portion of the film will be removed by masking and etching techniques to produce a smooth wedge. Then a portion of the specimen surface will be metallized across the wedge. The displacement of light interference fringes on crossing the wedge in the metallized and nonmetallized portions will be measured using optical interferometer. The fringe displacement in the metallized portion, p, and the fringe displacement in the nonmetallized portion, q, is related to the optical thickness of the film. The refractive index of the film is given by

$$1+q/p \qquad (3\ 3\ 1)$$

The thickness of the film is given by

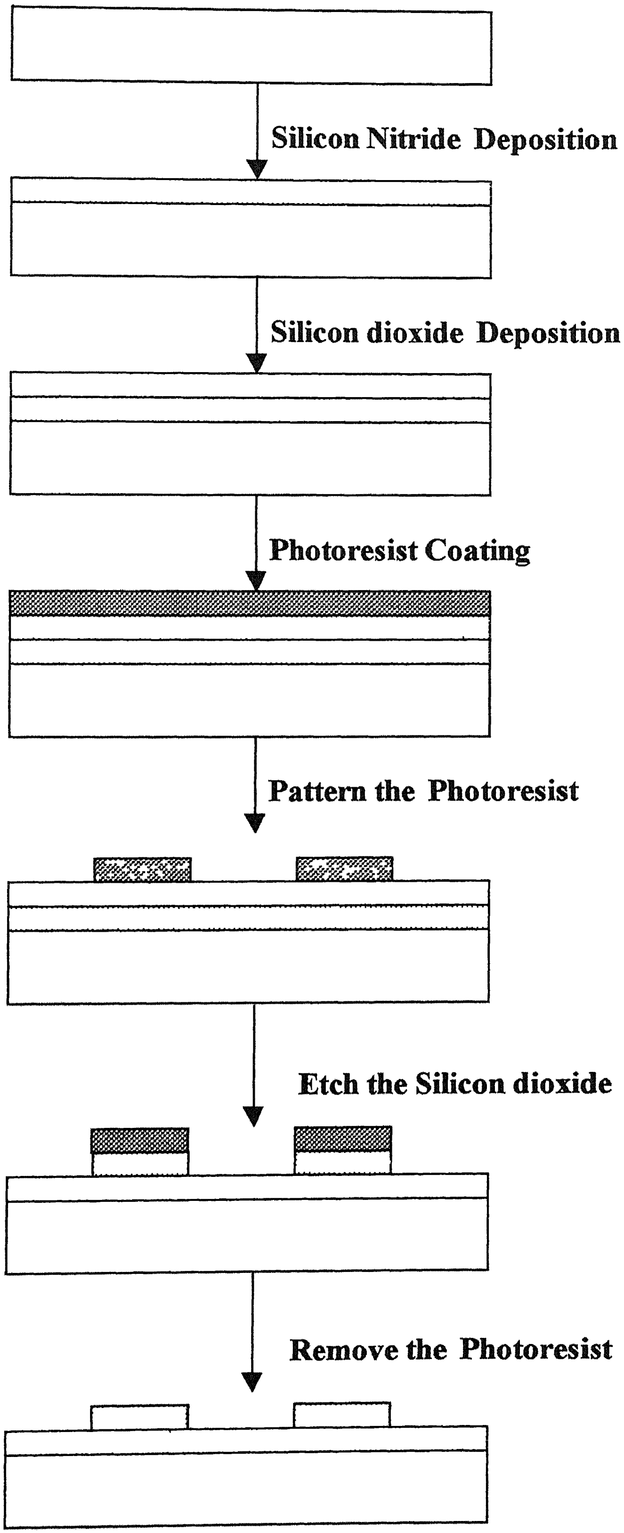
$$(P + dP)\lambda/2 \qquad (3.3.2)$$

Where 'P' is the number of fringes and dP is the fraction of fringe shift corresponding to the metallized portion and λ is the wavelength of light used. The sample preparation for these measurements is slightly involved, as the silicon nitride is difficult to pattern

3.3.1. Preparation of Silicon Nitride sample for refractive index measurement

As discussed above, that for measurement of refractive index of silicon nitride, it should be patterned. Silicon nitride can be patterned at 180^oC by phosphoric acid (H_3PO_4). If we keep photoresist as mask and patterning silicon nitride, then at 180^oC

photoresist wont be stable. So the solution is to deposit silicon dioxide on these silicon nitride films and pattern the silicon dioxide using photoresist and keeping this patterned silicon dioxide as a mask, silicon nitride film can be patterned. Flow chart for the preparation is shown below



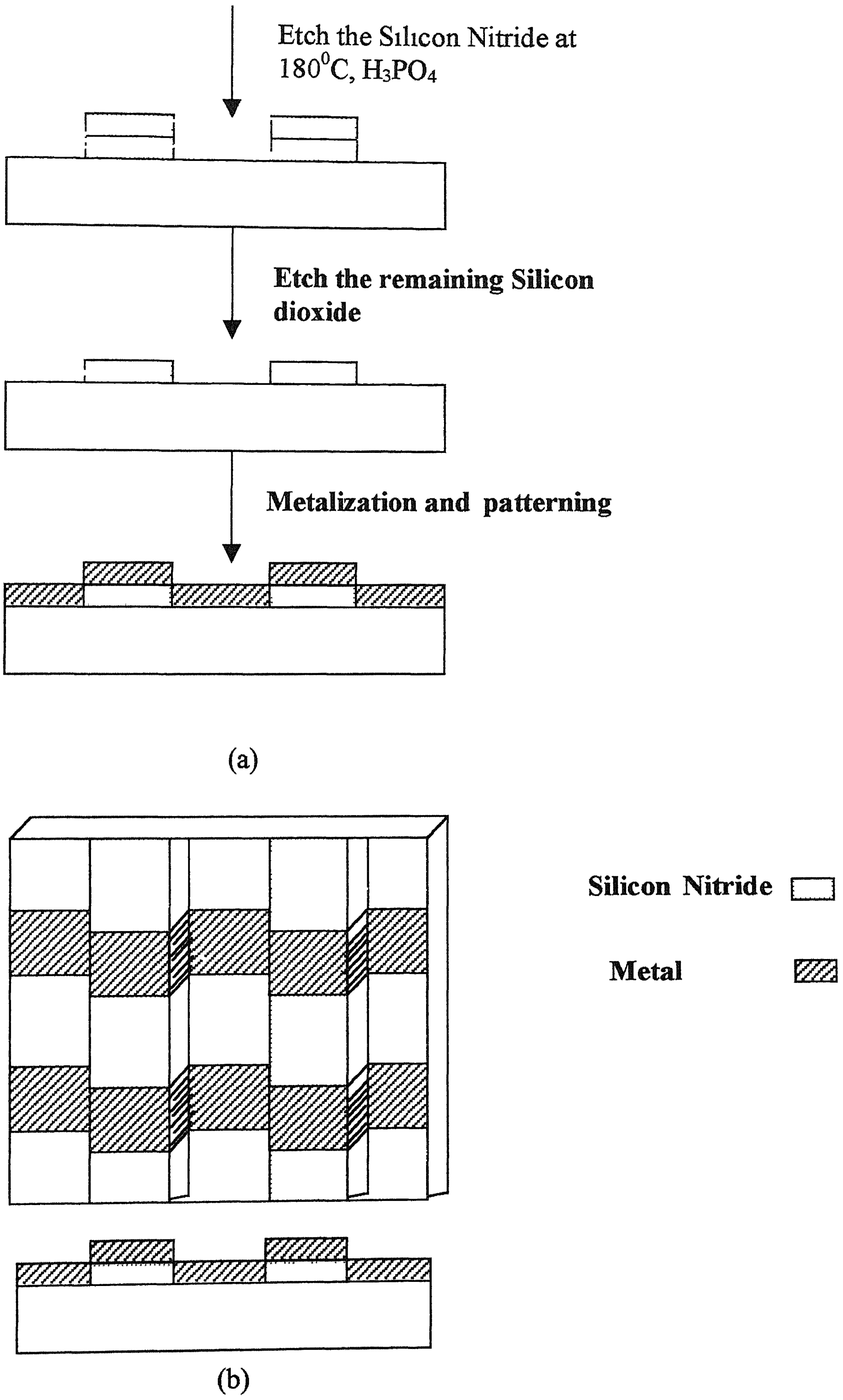

Etch the Silicon Nitride at 180^{0}C, H_3PO_4
Etch the remaining Silicon dioxide
Metalization and patterning
(a)
Silicon Nitride
Metal
(b)

Fig. 3.3.1 (a) Flow chart, (b) Top and side view of the prepared Silicon Nitride sample

3.4 Capacitance Voltage (CV) Measurement

CV measurement is a plot of capacitance of MIS capacitor as a function of its gate bias, which gives the dielectric constant of a material The measured MIS capacitor structure consists of silicon substrate, which can be either p or n-type covered by insulator(s) such as oxide or nitride or composite of these two and a metal electrode above. The cross section of MIS capacitor and CV measurement instrument is shown in the fig. 3.4.

Unlike MIS transistor, MIS capacitor is a two terminal device whose capacitance will vary with the applied gate to substrate voltage The capacitance verses voltage characteristics of MIS capacitors that result from the modulation of the width of the surface charge region by the gate voltage, have been found to be extremely useful in the evaluation of the electrical properties of insulator semiconductor interfaces. Here our interest is MNS capacitor (Silicon nitride insulator capacitor).

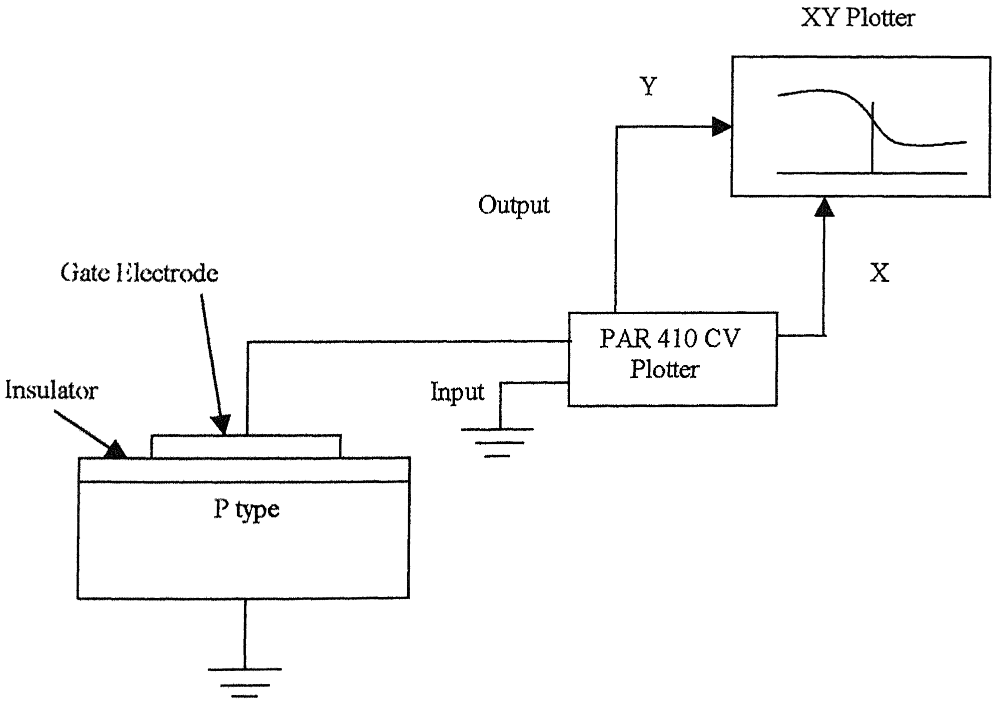


Fig. 3.4. CV measurement setup

3.4.1. Qualitative description of ideal MNS capacitor

There are 3 regions (depletion, accumulation & inversion) of interest when capacitance of MNS capacitor is plotted as a function of voltage The characteristics of thin oxide MNOS capacitor are also similar to MNS up to some voltage limit. In MNOS for higher voltages, tunneling of carriers through oxide takes place and charge trapped at the interface between oxide and nitride CV measurements were done on MNS capacitors to determine the dielectric constant of silicon nitride films deposited at various temperatures. The dielectric constant of a material is given by,

$$C_n\, T_n / A\, \varepsilon_o \tag{3.4.1}$$

Where C_n is capacitance of MNS capacitor. A is the area of the gate electrode and T_n is the thickness of the insulator (nitride). To understand the observed CV plots of MNS capacitors consider for the case of p-type substrate in the above discussed regions accumulation, depletion and inversion.

3.4.1.1 Accumulation

If we apply negative gate voltages, majority carrier holes will be attracted to the surface of the silicon to terminate the electric filed in the gate insulator; consequently, a p-type surface accumulation layer will be formed in the silicon, as shown in Fig. 3.4.1.1

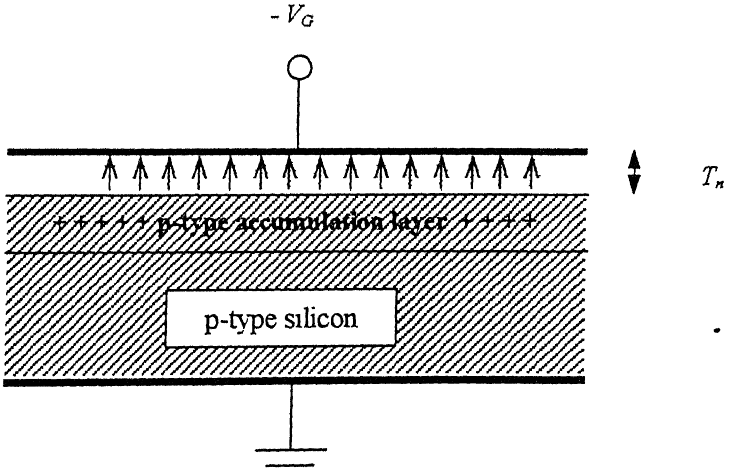


Fig. 3.4.1.1 Surface accumulation in MNS capacitor fabricated on p-type silicon substrate.

The high concentration of holes near the accumulated silicon surface can be thought of as forming the second electrode of a parallel-plate capacitor with the gate electrode. Since the accumulation layer is in direct Ohmic contact with the p-type substrate, the capacitance of the structure under accumulation conditions must be approximately equal to $\varepsilon\varepsilon_0 A/T_n$

3.4.1.2 Depletion

If the magnitude of applied voltage is decreased, the hole concentration at the surface of the silicon will also decrease. As this process continues, the gate voltage can eventually be reduced to the point where the surface hole concentration will go to zero and only a surface depletion region consisting of non mobile ionized acceptors will be required to terminate the electric field in the gate insulator, as is illustrated in Fig. 3.4.1.2

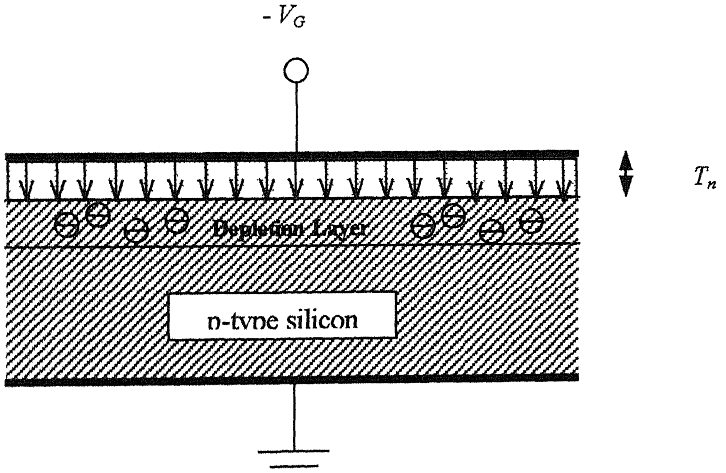


Fig. 3.4.1.2 Surface depletion in MNS capacitor

Since the magnitude of the charge density per unit area in the surface depletion region will be equal to the acceptor doping concentration times the width of the surface depletion region, increasingly positive gate-to-substrate voltage will tend to increase both depletion region charge (Q_{SD}) and width x_d. As the width of the depletion region, increasingly positive gate-to-substrate voltage will tend to increase both Q_{SD} and x_d As the width of the surface depletion region increases, the capacitance from gate to substrate associated with the MNS capacitor structure will decrease, because the capacitance associated with the surface depletion region will add in series to the capacitance across the gate insulator. Thus the total capacitance per unit area from gate to substrate under depletion conditions is given by

$$C(V_G) = \left(\frac{1}{C_n} + \frac{1}{C_{SD}(V_G)}\right)^{-1} \tag{3.4.2}$$

where C_n is the insulator capacitance per unit area, and C_{SD} is the capacitance per unit area associated with the surface with the surface depletion region.

3.4.1.3 Inversion

With the increase of positive applied voltage, the surface depletion region will continue to widen until the onset of surface inversion is observed as conduction band electrons are attracted up to the silicon surface to form an n-type inversion layer This situation is shown in Fig. 3.3.1.4

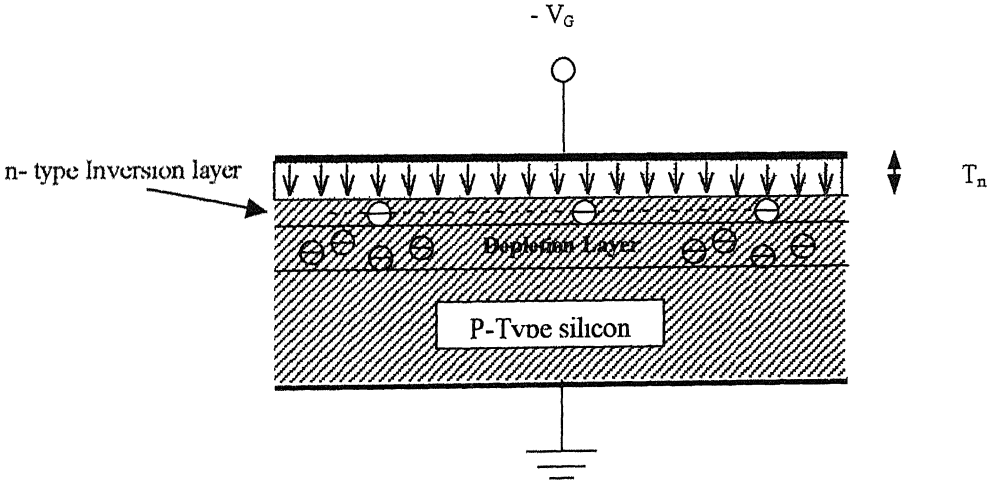


Fig. 3.4.1.3 Surface inversion of MNS capacitor

The width of the surface depletion region for a MNS structure in equilibrium will remain virtually constant after the formation of a surface inversion layer, even if the gate voltage is made more positive. Small variations in the width of the surface region around its maximum value can occur, however, if a nonequilibrium situation exists where the charge density in the inversion layer is unable to follow a high-frequency small-signal a.c.voltage applied to the gate electrode, superimposed on the d.c. bias. Since the charge density in the inversion layer may or may not be able to follow the capacitance under inversion conditions will be a function of frequency In general, when a surface inversion layer is present, the gate-to-substrate capacitance of the MNS capacitor structure, for low-frequency a.c.signals (less than few hundred Hertz), will be equal to the dielectric capacitance. For high-frequency signals, the observed capacitance will be equal to the series combination of the dielectric capacitance and the capacitance associated with the surface depletion region at its maximum width.

The following Fig.3.4.1.4 and Fig 3.4.1.5 shows the capacitance versus voltage relationships for MIS capacitors fabricated on p-type and n-type silicon substrates respectively, both high frequency and low frequency.

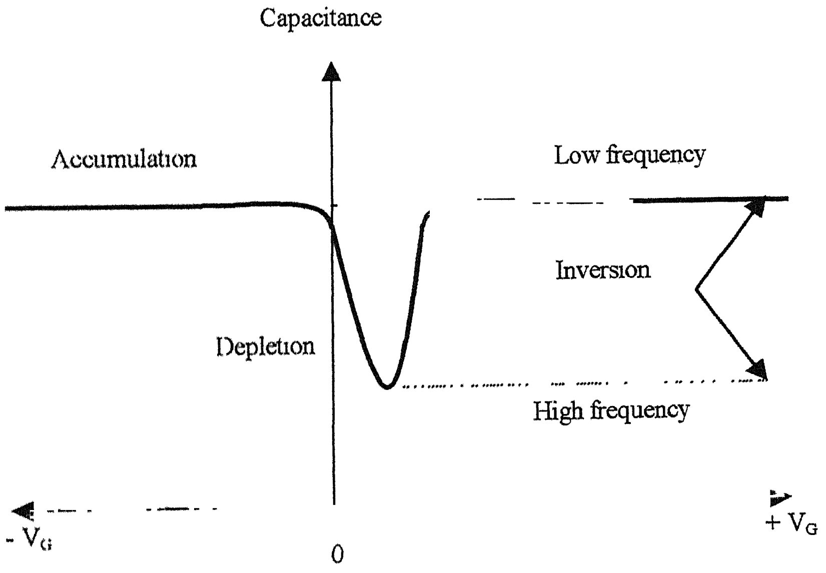


Fig. 3.4.1.4 CV Plots of MIS Capacitor fabricated on p-type substrate

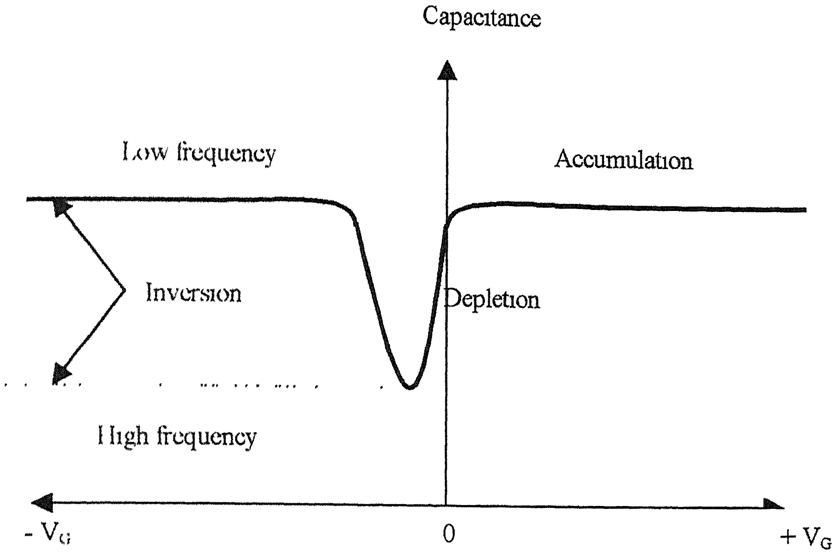


Fig. 3.4.1.5 CV Plots of MIS Capacitor fabricated on n-type substrate

3.4.2 CV plots of MNOS capacitors

The CV behavior of thin oxide MNOS capacitor is similar to MNS capacitor for small gate bias voltages. For higher gate bias voltages, charge tunnels from the thin silicon dioxide and will be trapped at the nitride, oxide interface. This will shift the CV plots of MNOS capacitor. The memory behavior can be noticed by observing the shift of the CV plots by application of gate voltage. Fig. 3.4.2 & Fig. 3.4.3 shows the CV behavior of MNOS capacitors.

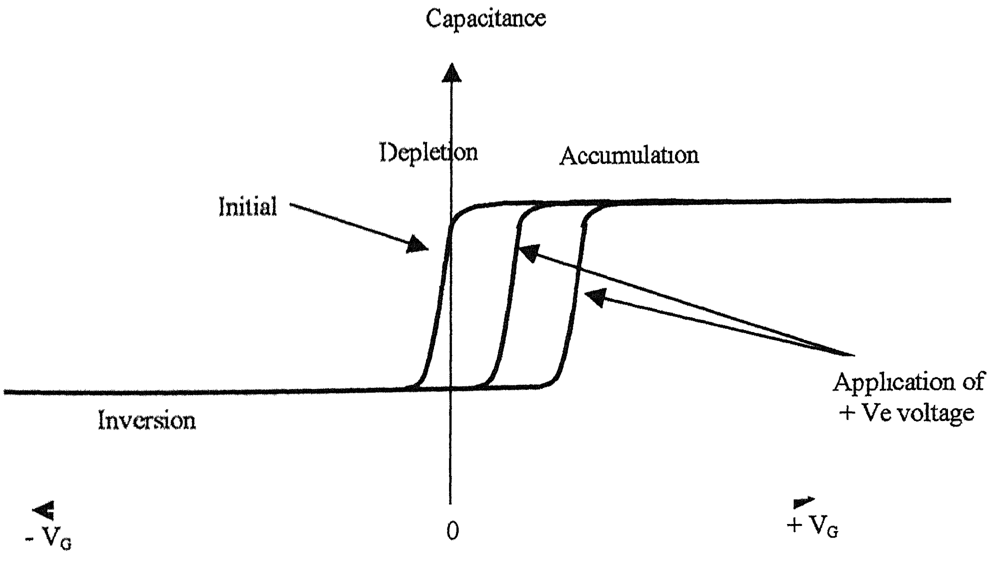


Fig. 3.4.2 CV plots of MNOS capacitor (n-type substrate)

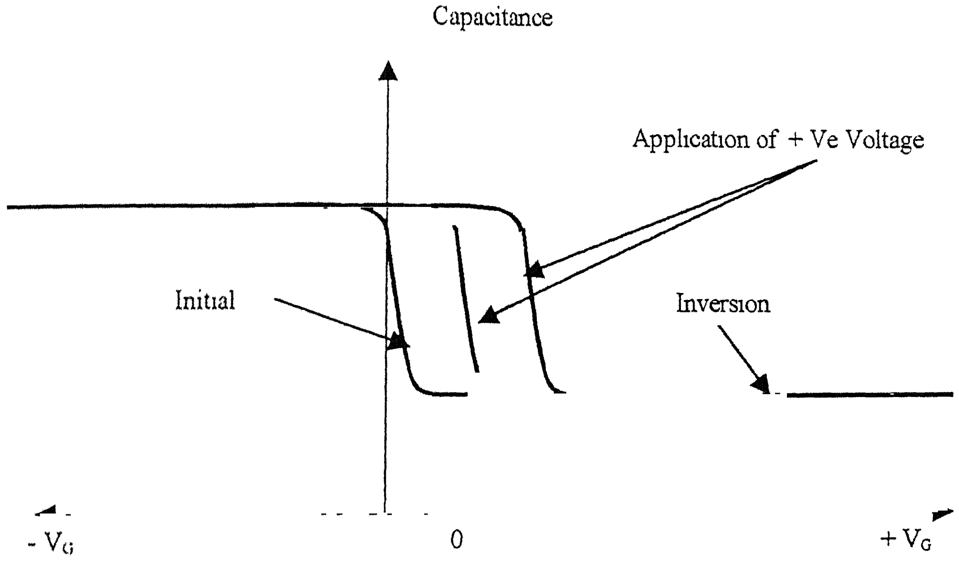


Fig. 3.4.3 CV plots of MNOS capacitor (p-type substrate)

These shifted CV curves can be returned back by applying appropriate D C gate bias voltages.

Chapter 4

4. MNOS Device Fabrication

MNOS transistors and capacitors have been fabricated on both p type and n type (100) wafers Four-mask process was planned to fabricate the transistors. The fabrication procedure is similar to the fabrication of MOS field effect transistors, except the insulator. The material, technology and process flow is given in the following sections. The layout of the transistor structure is shown in Fig 4.6 in section 4 3 below. The source diameter is 75μm. Drain annular length is 75 μm and the gate length is 20 μm.

Before starting the transistor fabrication, one has to prepare the required masks. The procedure for the preparation of the masks is given below,

4.1 Procedure for Preparation of masks

As discussed above, four-mask process was planned to fabricate the transistors. First mask for source and drain opening. Second mask for gate opening. Third mask for metal contact opening and finally the fourth mask for patterning of the deposited metal.

At first 100 times large drawings of final pattern size (all the four) are drawn on the Graph paper and then the same is transformed on rubylith using coordinatograph. Next this pattern is illuminated and reduced 20 times in size to form a glass reticle mask, using camera. This mask consists of a polished glass plate, coated with a high-resolution, orthochromatic emulsion, about few μm thick This emulsion is high sensitive to red light, so that a high contrast pattern can be replicated in it after exposure and developing in developer and hardener solutions. This is called first reduction. Second reduction is done on the other reticle in which the size is further reduced by 5 times. Then, using step and repeat camera a matrix of 5 X 10 patterns made on the other reticle. Matrix of patterns prepared on the masks to make multiple devices which is useful when one device fails in the processing or some other way other devices are become useful Fig. 4.1.1 shows the flow chart for reticle mask making.

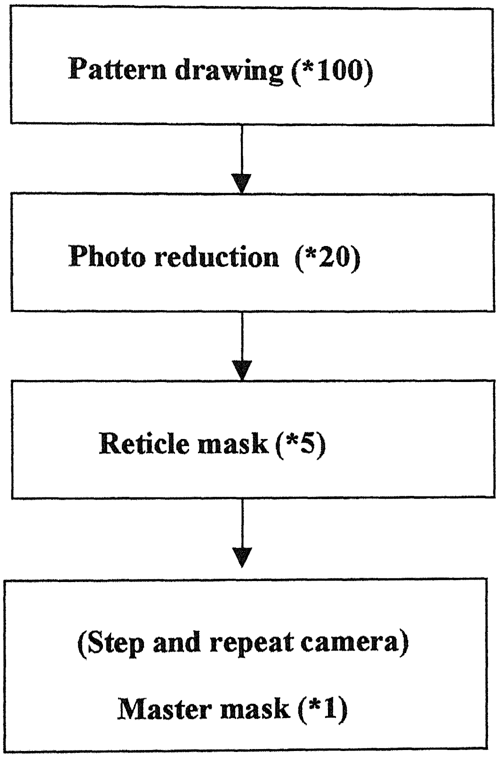


Fig. 4.1.1 Flow chart for mask making

The prepared masks are

Mask 1: For source and drain opening. The source diameter is 150 μm and drain annular ring of thickness 150 μm.

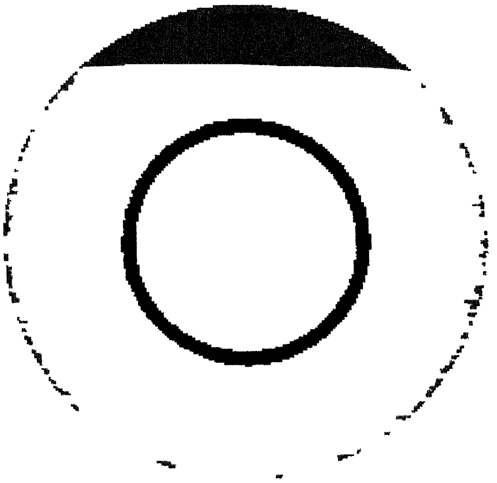


Fig. 4.1.2 Mask 1

Mask 2: For gate opening. The gate annular ring thickness is 30 μm. The gate is opened 5 μm inside in both the source and drain.

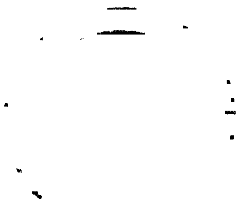


Fig. 4.1.3 Mask 2

Mask 3: Metal contact opening. The source opening diameter is 75 μm and drain annular ring opening thickness is 75 μm

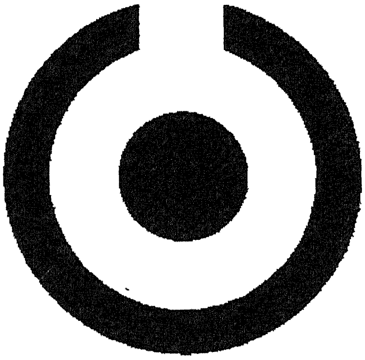


Fig.4.1.4 Mask3

Mask 4: For patterning of the deposited metal. The source metal diameter is and drain annular ring thickness 75 μm and gate annular metal ring thickness is 20 μm.

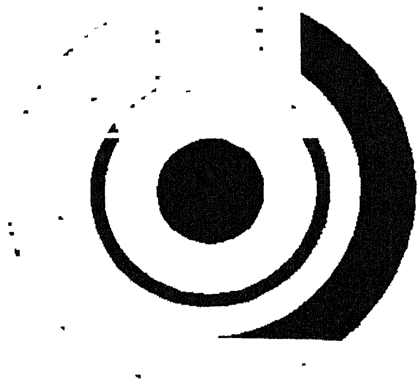


Fig.4.1.5 Mask 4

4.1.1 Photolithographic Process

Selective etching of thin films can be done by photolithographic process. The following Fig. 4 1.1.1 represents the flow chart for selective etching of the films by photolithographic process

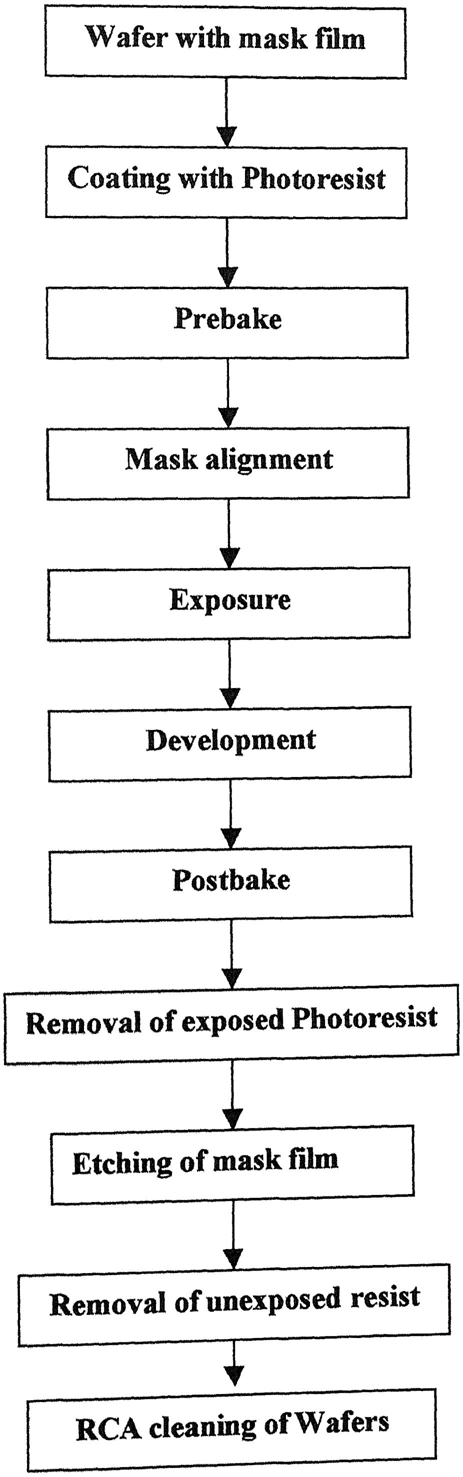


Fig. 4.1.1.1 flow chart for Photolithographic process

4.2 Raw material

Two different types of n-type and p-type (100) silicon wafers separately used for fabrication of MNOS capacitors and transistors. The information is given below.

For transistor:

n-type wafers.

Resistivity 5-10 Ω-*cm*

Substrate Thickness 350 ±20 μm

p-type wafers:

Resistivity 4-11 Ω-*cm*

Substrate Thickness 350 ±20 μm

For capacitors:

nn^+ epitaxial

Resistivity 3.4-4. Ω-*cm*

Phosphorous doped Epi thickness 15 μm

Substrate Resistivity 0.0015 Ω-*cm*

Substrate Thickness 350 ±20 μm

pp^+ epitaxial

Resistivity 8-11. Ω-*cm*

Boron doped Epi thickness 15 μm

Substrate Resistivity 0.0015 Ω-*cm*

Substrate Thickness 350 ±20 μm

4.3 MNOS Capacitor fabrication

Initially MNOS capacitors were fabricated by wet oxidation of silicon on both p-type and n-type (100) wafers. And again these devices were fabricated by dry oxidation of silicon on both n type and p-type (100) wafers The fabrication processing flow chart is given below.

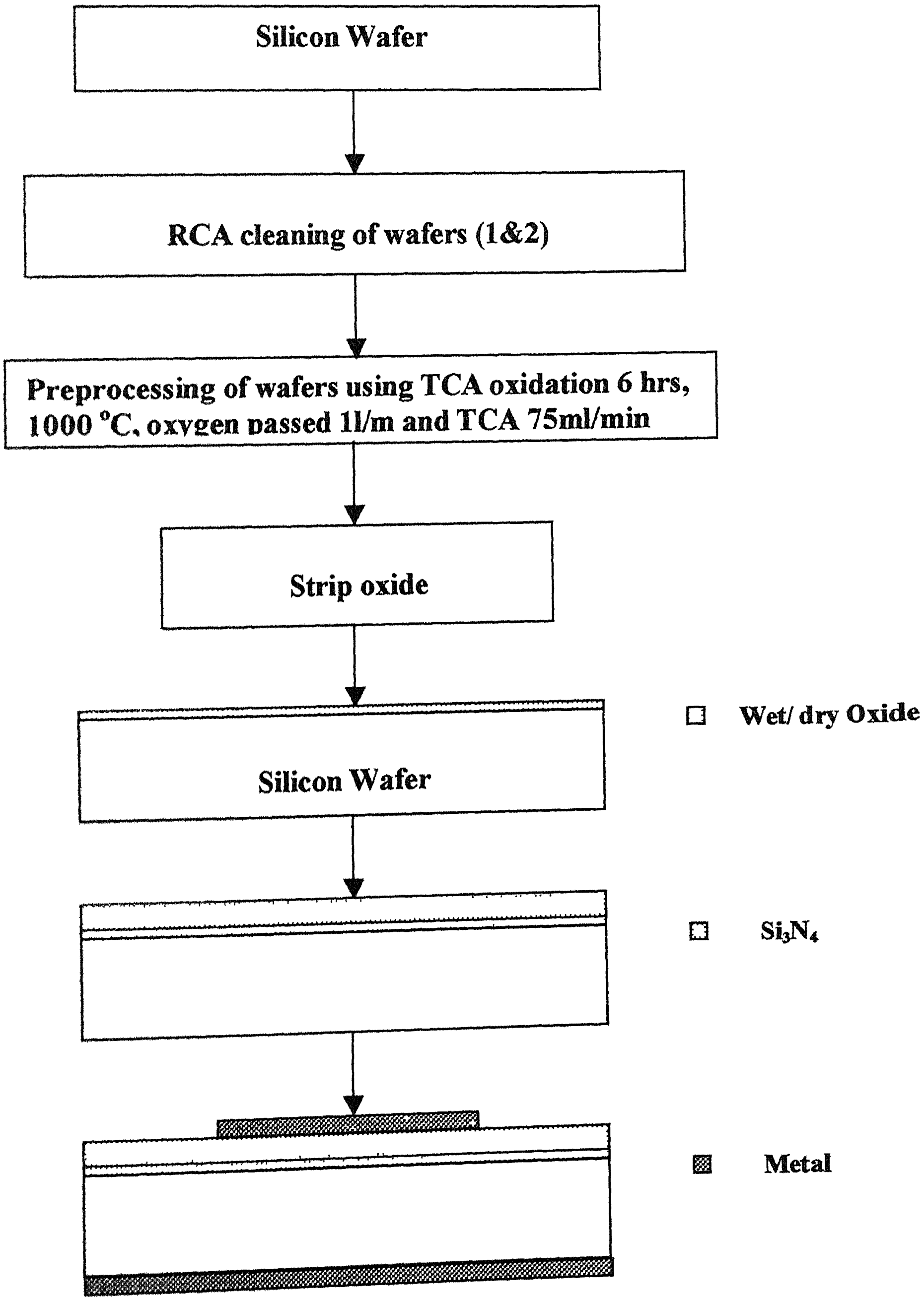
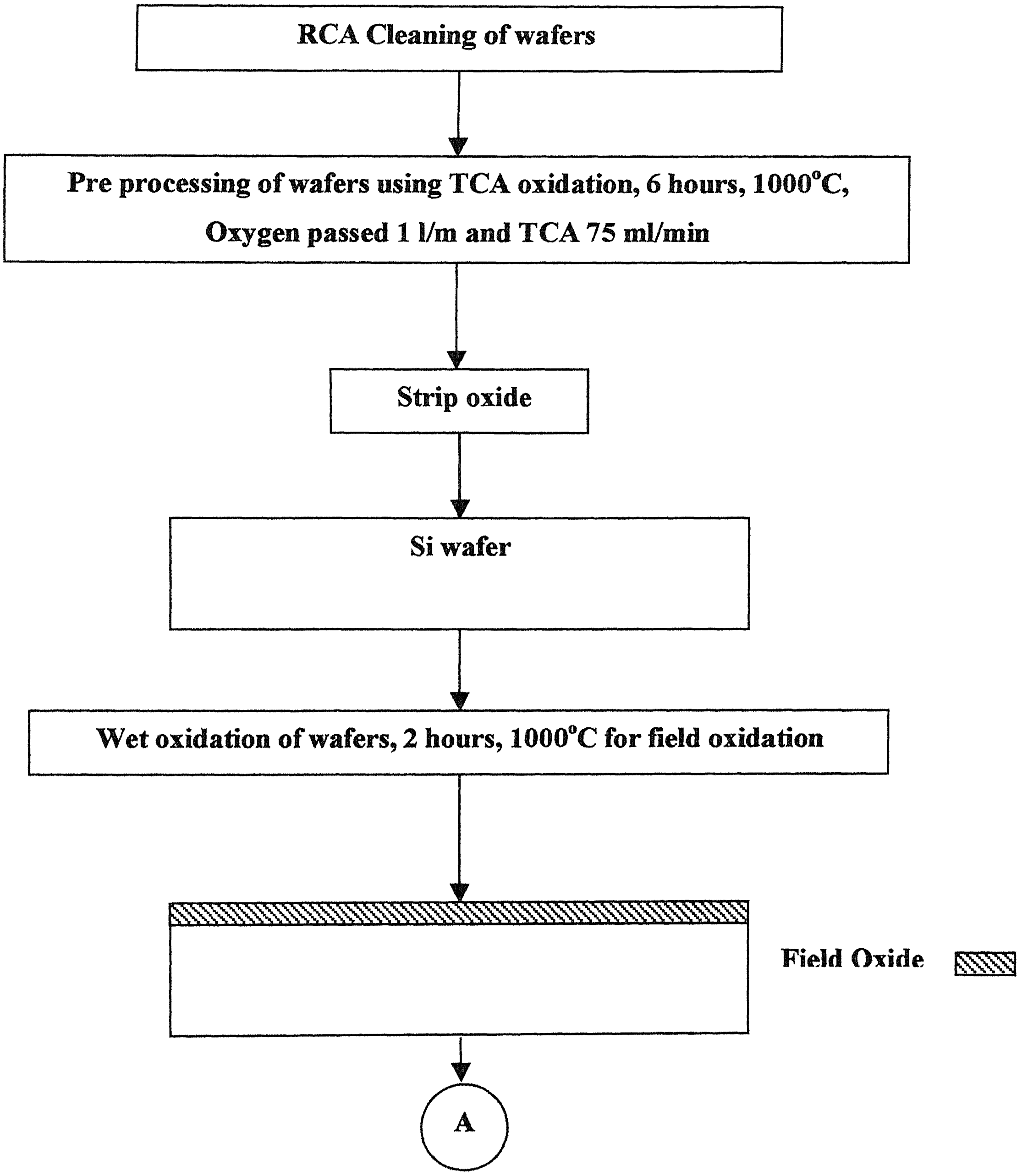

Silicon Wafer
RCA cleaning of wafers (1&2)
Preprocessing of wafers using TCA oxidation 6 hrs, 1000 °C, oxygen passed 1l/m and TCA 75ml/min
Strip oxide
Silicon Wafer
☐ Wet/ dry Oxide
☐ Si_3N_4
▨ Metal

Fig. 4.3.1 Process flow chart for fabrication of MNOS capacitor

4.4 Transistor Fabrication

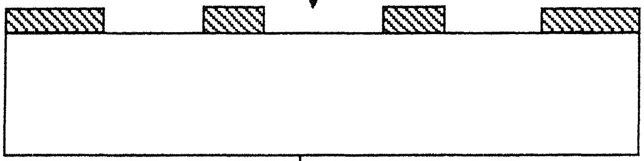
Initially the transistors were fabricated only on p-type wafers. For gate oxide wet oxidation was done. Then silicon nitride was deposited at 750°C Later again transistors were fabricated on both p-type and n-type wafers. This time for gate oxide, dry oxidation was done. The processing flow chart is shown below

Process Flow chart


RCA Cleaning of wafers
Pre processing of wafers using TCA oxidation, 6 hours, 1000°C, Oxygen passed 1 l/m and TCA 75 ml/min
Strip oxide
Si wafer
Wet oxidation of wafers, 2 hours, 1000°C for field oxidation
Field Oxide ▨
A

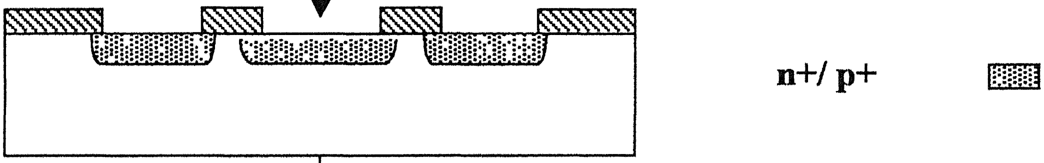
A

Photolithography for 1st mask for n^+ or p^+ for source and drain window open.



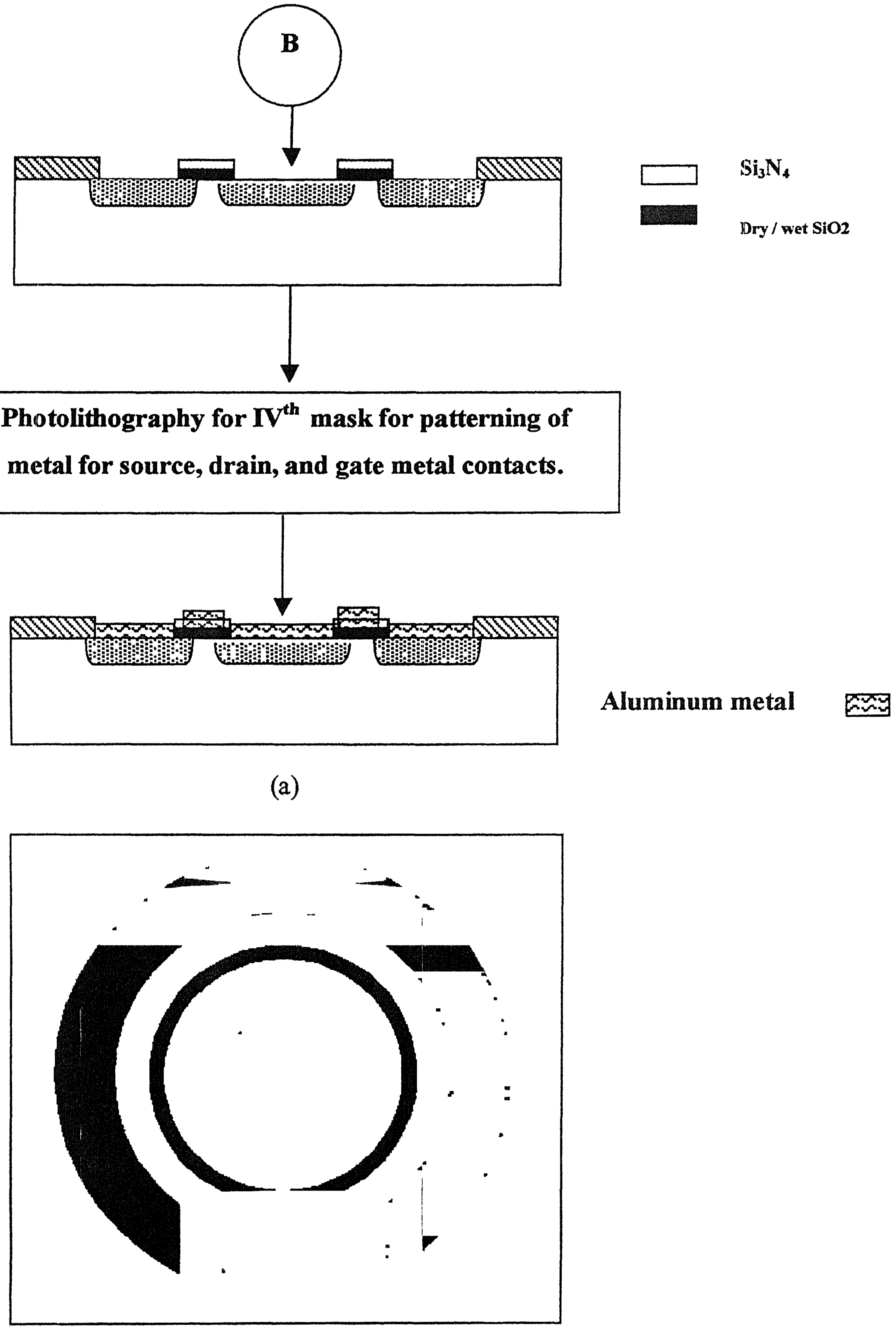
In case of p-type wafers: for source and drain n^+, $POCl_3$ deposition at 950°C, 30 min and drive in at 1000°C, sheet resistivity, $R_s = 27.5$ Ω/sq for p-type wafers.

In case of n-type wafers: for source and drain p^+, boron doped oxide by CVD using tri-propyle-borate and TEOS by pyrolytic decomposition at 660°C, soak-in, removal of doped oxide and drive in 20 min.



Photolithography for IInd mask for gate opening

B


B
Si3N4
Dry / wet SiO2
Photolithography for IVth mask for patterning of metal for source, drain, and gate metal contacts.
Aluminum metal

(a)

(b)

Fig. 4.6 (a) Flow chart for fabrication of MNOS transistor (b) Top view of the transistor designed

Chapter 5

5. Results and Discussion

Once the silicon nitride reactor is assembled, next step is deposition of silicon nitride and its optimization. So at different temperatures and different flow rates of the reactants silicon nitride deposition has been carried out. The composition of the films deposited at different temperatures was checked by RBS measurement, chemical nature was studied by IR measurement, dielectric constant was measured by CV measurement and refractive index measurement was carried out using interference measurement. And once the deposition was optimized then MNOS devices (capacitors & Transistors) were fabricated on both the P-type and N-type wafers.

5.1 Silicon Nitride deposition

In APCVD reactor the variables to control the deposition and the film properties is only by varying the temperature and flow rates of the reactants. To optimize the silicon nitride deposition of the reactor, the temperature of the reactor was fixed and varied the flow rates of dichlorosilane and Ammonia. Then same procedure was followed at different temperatures. The experiments were carried out in the temperature range of 700 to 900°C. But the deposition has started at temperature 750 °C. Good quality, adherent and uniform films were noticed in temperature range of 750 to 850 °C. At temperatures 900 °C and above, a very high nonuniformity and haziness were noticed in the deposited films. The following table 6.1 summarizes the deposition characteristics of silicon nitride films deposited at various deposition conditions. The dichlorosilane was diluted with nitrogen by connecting another nitrogen line to this and passed to the reactor chamber to avoid blockage in the tube, as dichlorosilane is very reactive. In the table N_2^* represents the flow rate of nitrogen mixed to dilute the dichlorosilane.

Temp (°C)	SiH_2Cl_2 flow rate (ml)	NH_3 flow rate (ml)	N_2 flow rate (ml)	N_2^* flow rate (ml)	Deposition	Remarks
700	15	500	1000	-	No	-
	25	500	1000	-	No	-
	30	500	1000	-	No	-
	35	500	1000	-	No	-
750	10	500	1000	-	Yes	Uniform deposition
	10	500	1000	400	Yes	Non uniform deposition (gradient)
	10	500	1000	500	Yes	Uniform deposition
	10	500	1000	600	Yes	Slightly non uniform deposition sides
	15	500	1000	-	Yes	Uniform deposition
	15	800	1000	500	Yes	Slightly non uniform deposition at sides
	15	500	1300	500	Yes	Flow like features
	15	500	1500	500	No	-
	15	1000	1000	500	No	-
	15	500	1000	500	Yes	Uniform deposition
	15	600	1000	500	Yes	Uniform deposition
	20	500	1000	-	Yes	Uniform deposition
	20	500	1000	500	Yes	Uniform deposition
	25	500	1000	-	Yes	Nonuniform deposition towards exhaust side
	30	500	1000	500	Yes	Nonuniform deposition
	35	500	1000	500	Yes	Nonuniform deposition
	35	700	1000	-	Yes	Highly Non uniform (deposition more at sides)
	55					
800	15	500	1000	-	No	
	20	500	1000	-	Yes	Uniform deposition
	25	500	1000	-	Yes	Uniform deposition
	30	500	1000	-	Yes	Nonuniform deposition through out the wafer

	35	500	1000	-	No	-
850	10	500	1000	-	No	-
	15	500	1000	-	Yes	Uniform deposition
	15	500	1000	500	Yes	Uniform deposition
	15	600	1000	500	Yes	Uniform deposition
	20	500	1000	-	Yes	Uniform deposition
	20	500	1000	500	Yes	Uniform deposition
	20	600	1000	500	Yes	Slightly non uniform deposition
	20	800	1000	500	No	-
	25	500	1000	-	Yes	Uniform deposition
	25	500	1000	500	Yes	Nonuniform deposition
	30	500	1000	500	Yes	Uniform deposition
	35	500	1000	-	Yes	Highly non uniform deposition -
	40	500	1000	-	Yes	Highly non uniform deposition (ripple like features)
	45	500	1000	-	Yes	Highly nonuniformity
	60	500	1000	-	No	-
	70	500	1000	-	No	-
900	20	500	1000	-	Yes	Nonuniformity and Haze
	25	500	1000	-	Yes	Highly nonuniformity and Haze

Table 5.1 deposition characteristics of silicon nitride at various deposition conditions

At temperature 700 °C the flow rates of ammonia and dichlorosilane were changed and tried for deposition and no deposition was noticed. At 750 °C deposition was noticed and by varying the dichlorosilane and ammonia flow rates the deposited film characteristics were observed. It was observed that as the temperature increases the deposition rate also increases. Fig. 5.1.1 show the variation of deposition rate with increase in temperature for a fixed dichlorosilane, ammonia and nitrogen flow rates.

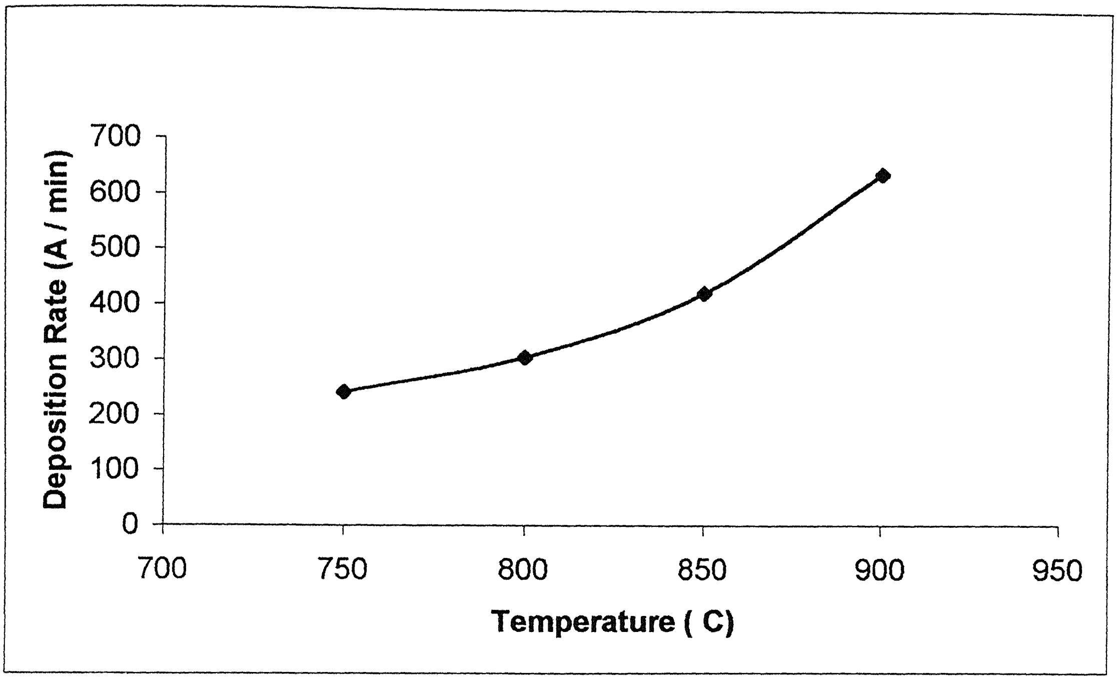


Fig. 5.1.1 Variation of deposition rate with temperature at constant dichlorosilane, ammonia and nitrogen flow rates of 20ml/min, 500ml/min and 1 lit/min respectively.

For low dichlorosilane flow rates, uniform silicon nitride deposition was noticed and as increasing the dichlorosilane flow rate deposition rate has also increases. As the dichlorosilane flow rates increases above 50 ml/min at 750 °C keeping ammonia and nitrogen flow rates at 500 mil/min and 1000 ml/min respectively, nonuniformity has been observed in the deposited films. The same thing is also observed at 800 °C and 850 °C for dichlorosilane flow rates of 60 ml/min and 70 ml/min respectively and keeping the same flow rates for ammonia and nitrogen. The Fig.5.1.2 & 5.1.3 show the variation of silicon nitride deposition rate with increase in dichlorosilane flow rate, keeping the ammonia and nitrogen flow rates constant at temperatures 750 °C and 850 °C.

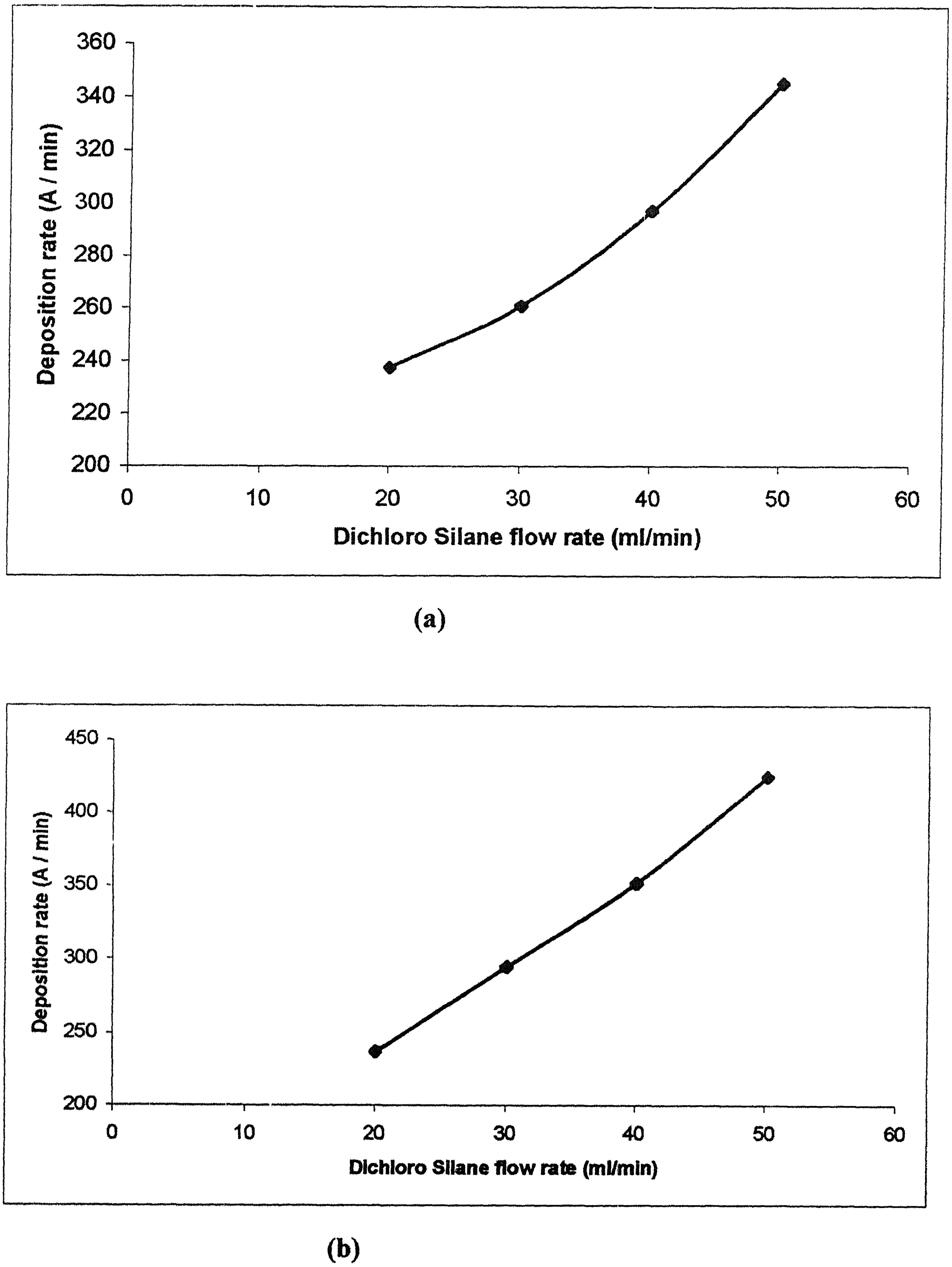
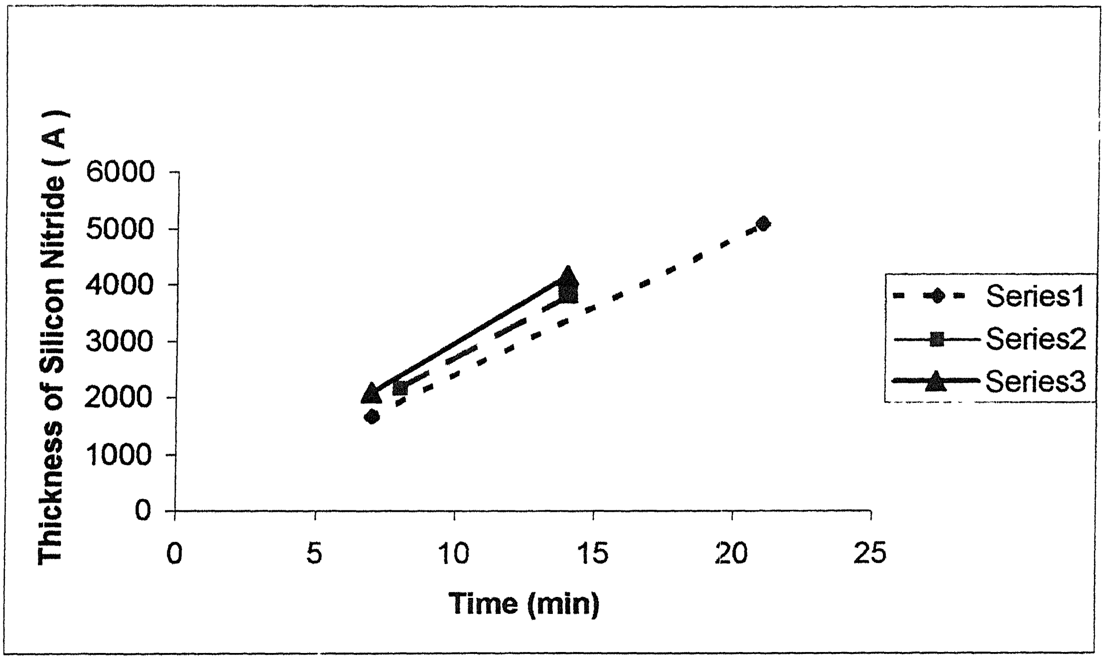
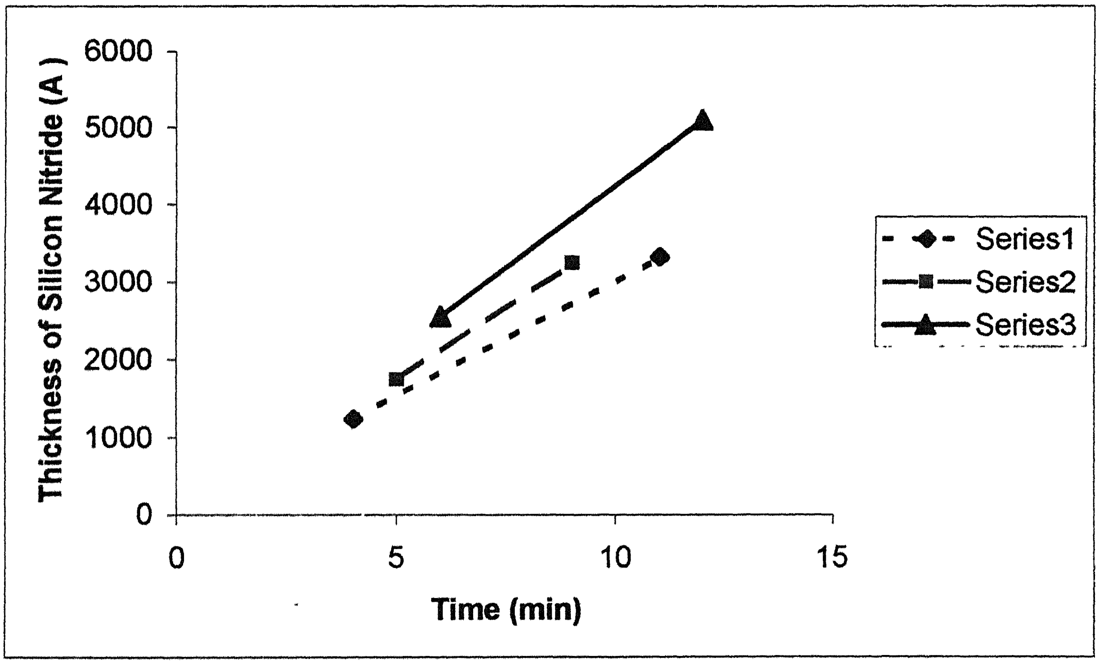


Fig.5.1.2 Variation of deposition rate with increase of dichlorosilane for a fixed Ammonia and nitrogen flow rates of 500 ml/min and 1 lit/min respectively at temperature (a) 750 °C and (b) 850 °C



(a)



(b)

Fig.5.1.3 Variation of Silicon Nitride thickness with Ammonia to dichlorosilane ratio Series 1 - 25, series 2 – 20, series 3 – 17 (a) 750 °C (b) 850 °C

As increasing the ammonia flow rate keeping constant dichlorosilane flow rate, the deposition rate increases slightly. For higher ammonia flow rates, nonuniformity has been observed. By further increasing the ammonia flow rate this nonuniformity is also increased. At ammonia flow rate of 1 lit/min and above no deposition is observed at all temperatures. It may be because of improper mixing of reacting gases. Keeping the dichlorosilane and ammonia flow rates constant and increasing the nitrogen flow rate, the deposition is slightly decreased with slight nonuniform deposition. As further increase of the nitrogen flow rate, the nonuniformity in the deposition was further increased in deposited films. With flow rates above 1500 ml/min, there was no deposition at all temperatures.

To observe the quality of deposited films, the films were etched in buffered HF. Fig 5.1.4 shows the variation of etch rate with deposition temperature. The deposited films are etched very fast in buffered HF due to the presence of high oxygen content and stresses in the films. It is observed that the etching rate of deposited films decreases with the increase in deposition temperature.

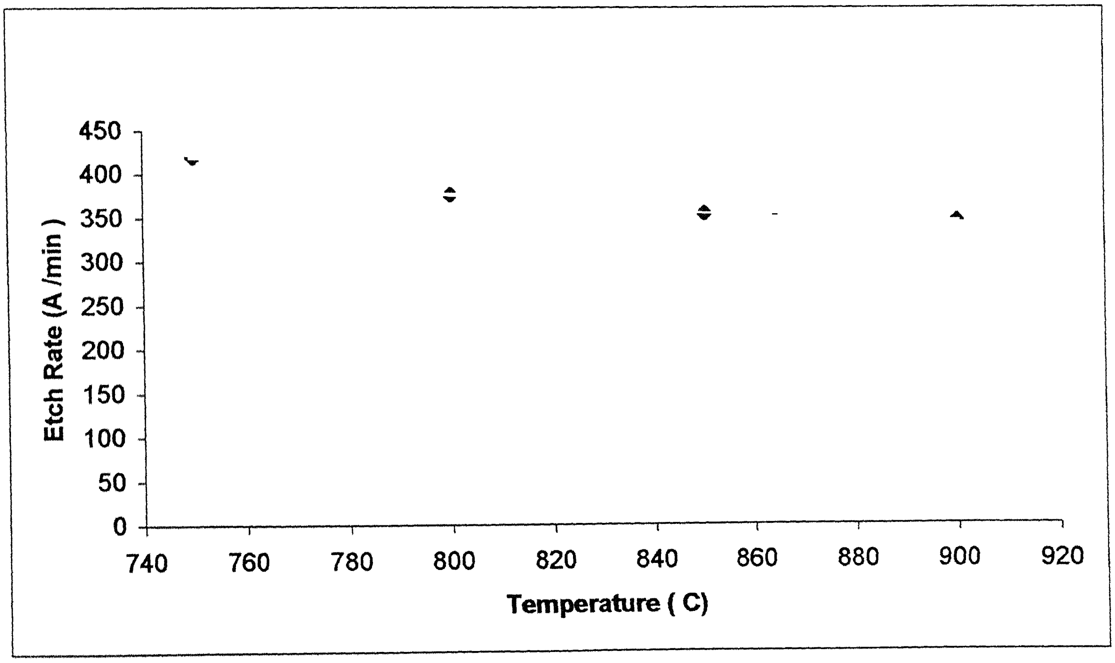


Fig. 5.1.4 Variation of Etch rate of the deposited silicon nitride films with Deposition Temperature.

The Dichlorosilane and ammonia used in our experiments were 99.99% pure so it is expected that the origin of oxygen in the deposited silicon nitride films is mainly due to the presence of oxygen in the supplying nitrogen. It has been verified when the nitrogen is passed through the liquid nitrogen trap, a high amount of oxygen is noticed in the trap. So to eliminate this oxygen in nitrogen in further experiments, the nitrogen is passed through the liquid nitrogen trap. The etching rate of the newly deposited films with this liquid nitrogen trap was decreased and after annealing the etching rate again further decreased. So the fast etching of the deposited films is not only due to the oxygen content and but also due to stresses in the film.

The annealing has been done at different temperatures. Fig5.1.5 & Fig 5.1.6 shows the variation of etching rate with deposition temperature after one hour annealing. As the annealing temperature increases the etching rate decreases and became saturated at higher annealing temperatures.

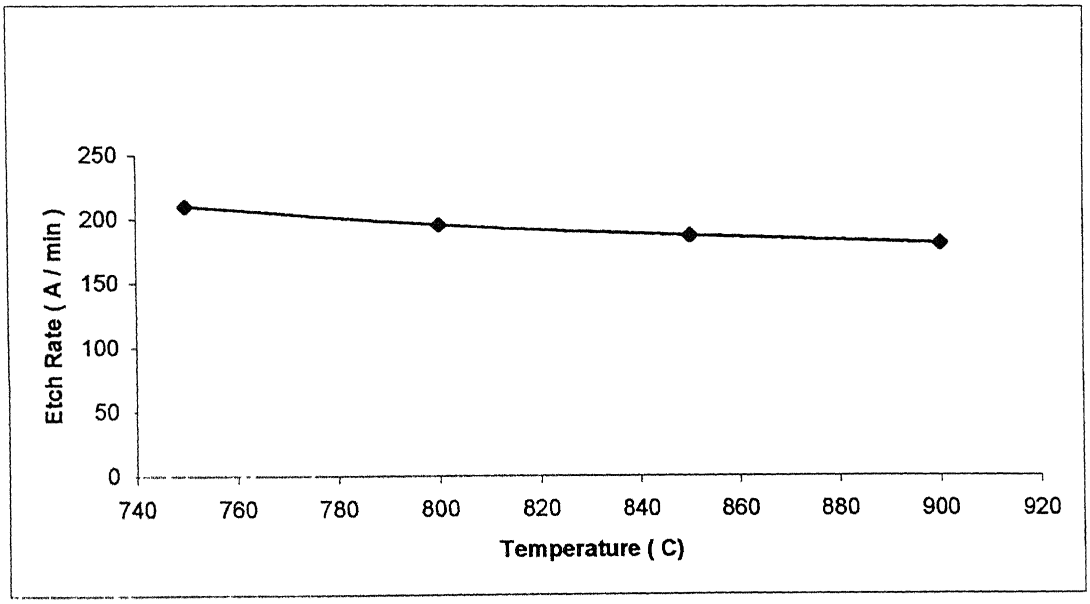
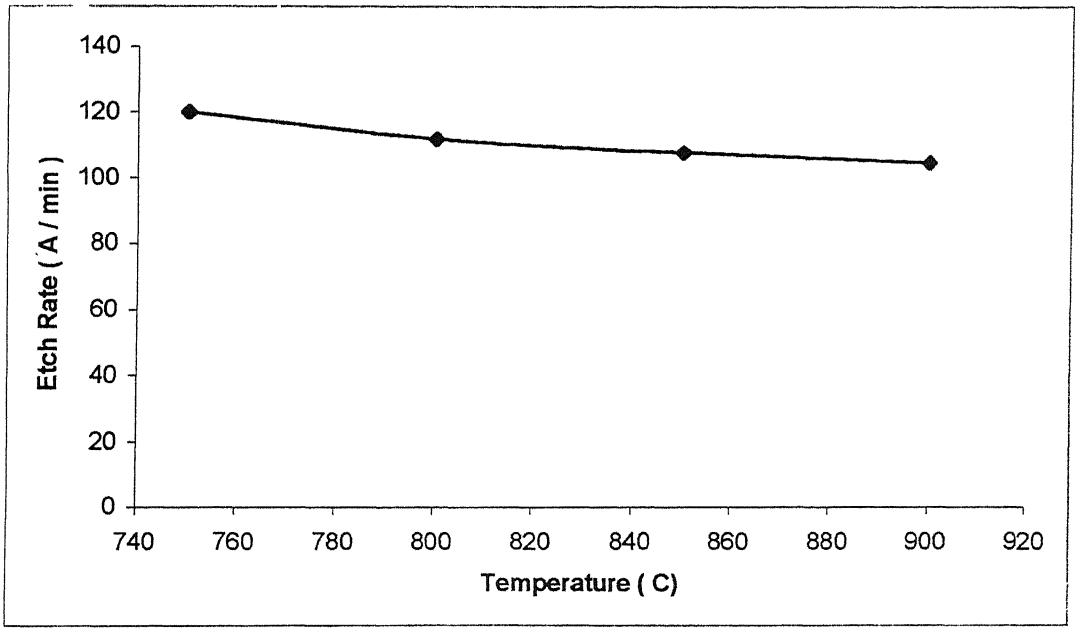
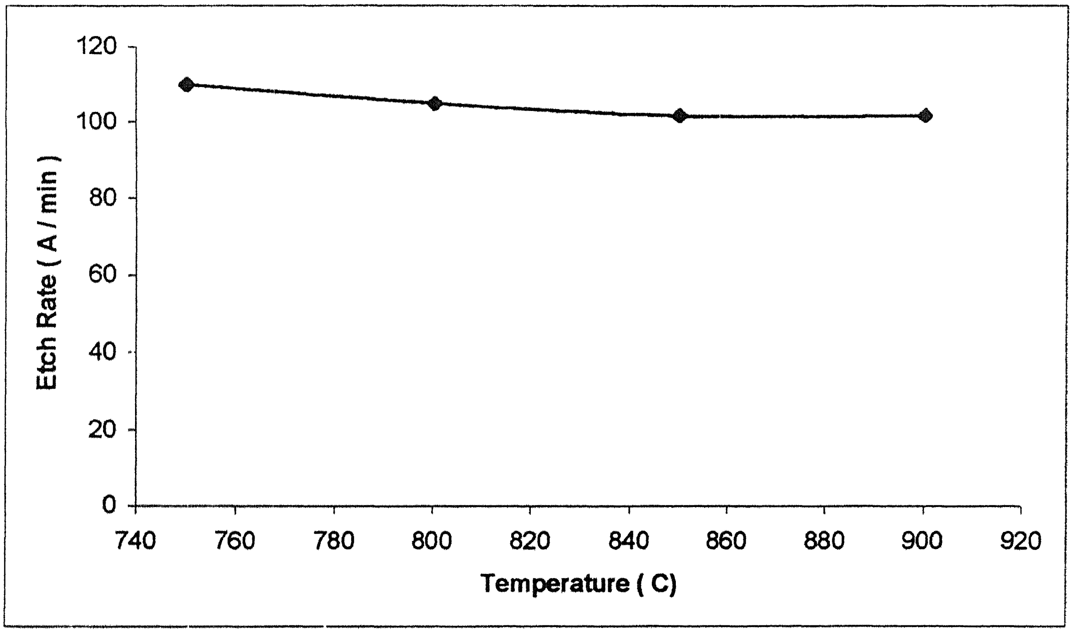


Fig. 5.1.5 Variation of Etch Rate with Deposition Temperature after one hour Annealing at 950 °C



(a)



(b)

Fig. 5.1.6 Variation of Etch Rate with Deposition Temperature after one hour Annealing at (a) 1000 °C and (b) 1050 °C.

After every deposition, ammonium chloride is deposited at the ends of the reactor tube, which is a by-product of the reaction. The films deposited without cleaning of this ammonium chloride observed with haziness For deposition of good quality films, proper cleaning of the tube is required after every run. If the ammonium chloride deposition is very low, then thorough cleaning of the reaction tube with TCE is recommended. If the ammonium chloride deposition is very high, then it is required to etch the tube by buffered HF.

The following Fig. 5.1.7, Fig. 5.1.8, and Fig. 5.1.9 are the films deposited at 750 °C, 800 °C and 850 °C for dichlorosilane, ammonia, and nitrogen flow rates of 20 ml/min, 500 ml/min, 1000 ml/min respectively. The deposition is uniform. Fig 5.1.10 represents the film deposited at 900 °C The deposition is non uniform and haziness is observed. In the figures the white color spots are ammonium chloride particulates. This cannot be completely eliminated, but can be minimized by maintaining high temperature at the ends of the tube.

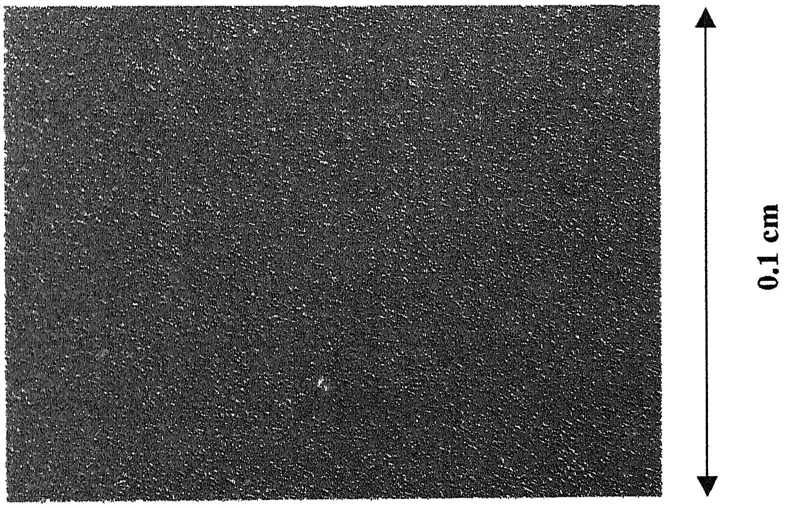


Fig 5.1.7 silicon nitride film deposited at 750°C

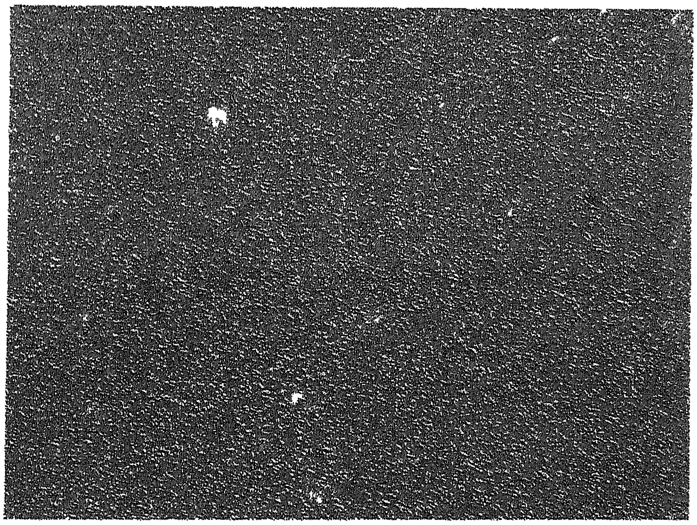


Fig 5.1.8 silicon film deposited at 800°C

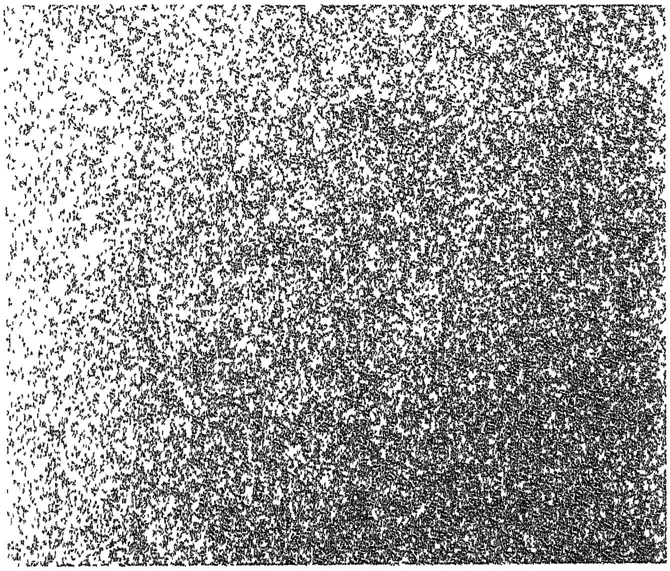


Fig 5.1.9 silicon nitride film deposited at 850°C

पुरुषोत्तम काशीनाथ केलकर पुस्तकालय
भारतीय प्रौद्योगिकी संस्थान कानपुर
अवाप्ति क्र० A. 139591

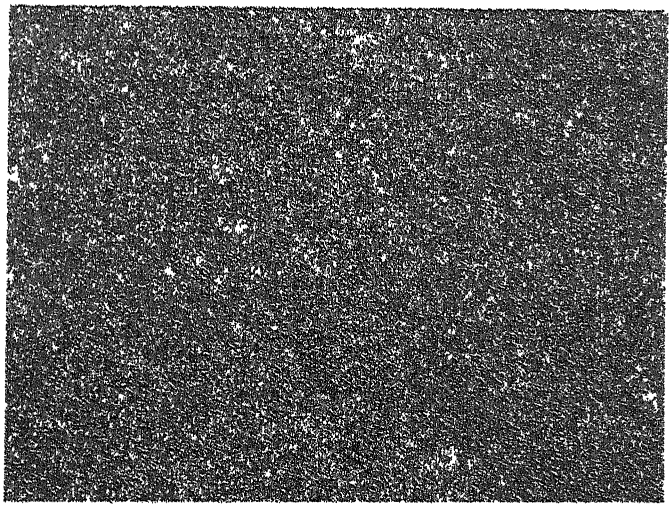


Fig 5.1.10 silicon nitride film deposited at 900°C

Cracks are observed on the films deposited thickness more than 5000 A°. In Fig 5.1.11 & Fig5.1.12 the cracks are clearly visible.

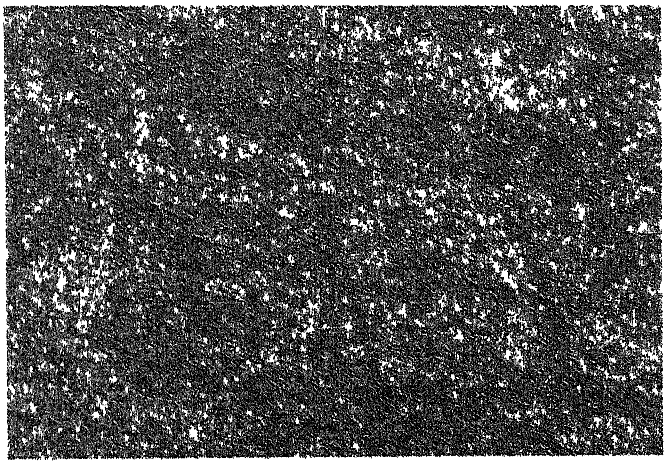


Fig 5.1.11 8000 A° film deposited at 900°C

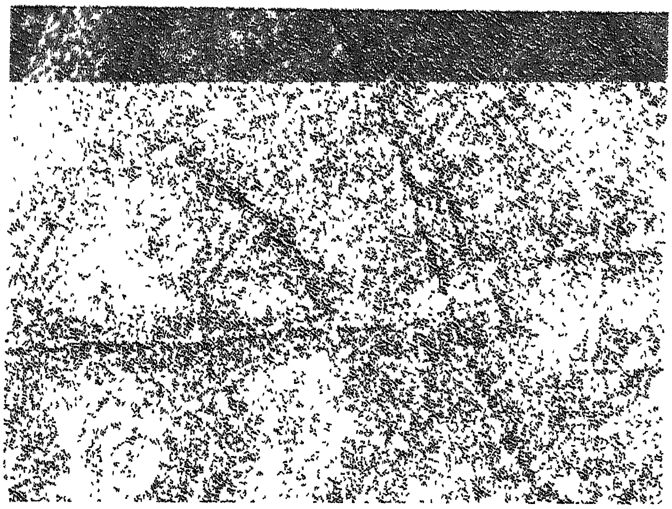


Fig 5.1.12 12000 A° film deposited at 900°C

5.2 RBS Measurement

From RBS, normalized yields versus channel or energy data is collected for different samples. Adjusting the nitride composition and the film thickness a simulation plot was also matched with experimental plot. Both the experimental and simulation plots for different samples are shown from the Fig.5.2.1 to Fig. 5.2.5. Silicon edge, oxygen edge and nitrogen edge are shown in the figures. Summary of RBS spectra for different samples is summarized below. The films deposited without liquid nitrogen trap in nitrogen line, show higher amount of oxygen. The samples prepared at different temperatures has been deposited by same dichlorosilane, ammonia and nitrogen flow rates of 20 ml/min, 500ml/min, 1000ml/min respectively. Measurements are made on the films deposited in the temperature range 750 – 900 °C.

Sample No	Temperature (°C)	Composition	Simulated Thickness (nm)	Measured Thickness
1	750	$Si_3N_4O_1$	170	155
2	800	$Si_{3.7}N_4O_{1.5}$	430	405
3	850	$Si_3N_4O_{0.5}$	510	490
4	900	$Si_5N_{1.5}O_1$	800	-
5	850	$Si_3N_4O_{0.2}$	850	-

Table 5.2 Composition and simulated thickness obtained from RBS measurement and physical thickness obtained from the interferometer measurement.

The fifth sample in the table is deposited, when the nitrogen is passed through liquid nitrogen trap to the reactor chamber. The oxygen content at the temperature 850 °C is decreased 0.5 to 0.2. From this we can clearly say that the origin of oxygen content in the film is mainly due to the nitrogen gas used. Fig.5.2.6 shows the variation of silicon to oxygen and silicon to nitrogen ratios with deposition temperature. It is observed that as the deposition temperature increases the silicon richness in the films is also increases except at temperature 850 °C. The silicon to oxygen ratio initially decreased with increase of temperature and above 850 °C it is increased with increase of temperature. The films deposited at temperatures 750 °C and 850 °C has the composition Si_3N_4. The physical thickness is measured by optical interferometer.

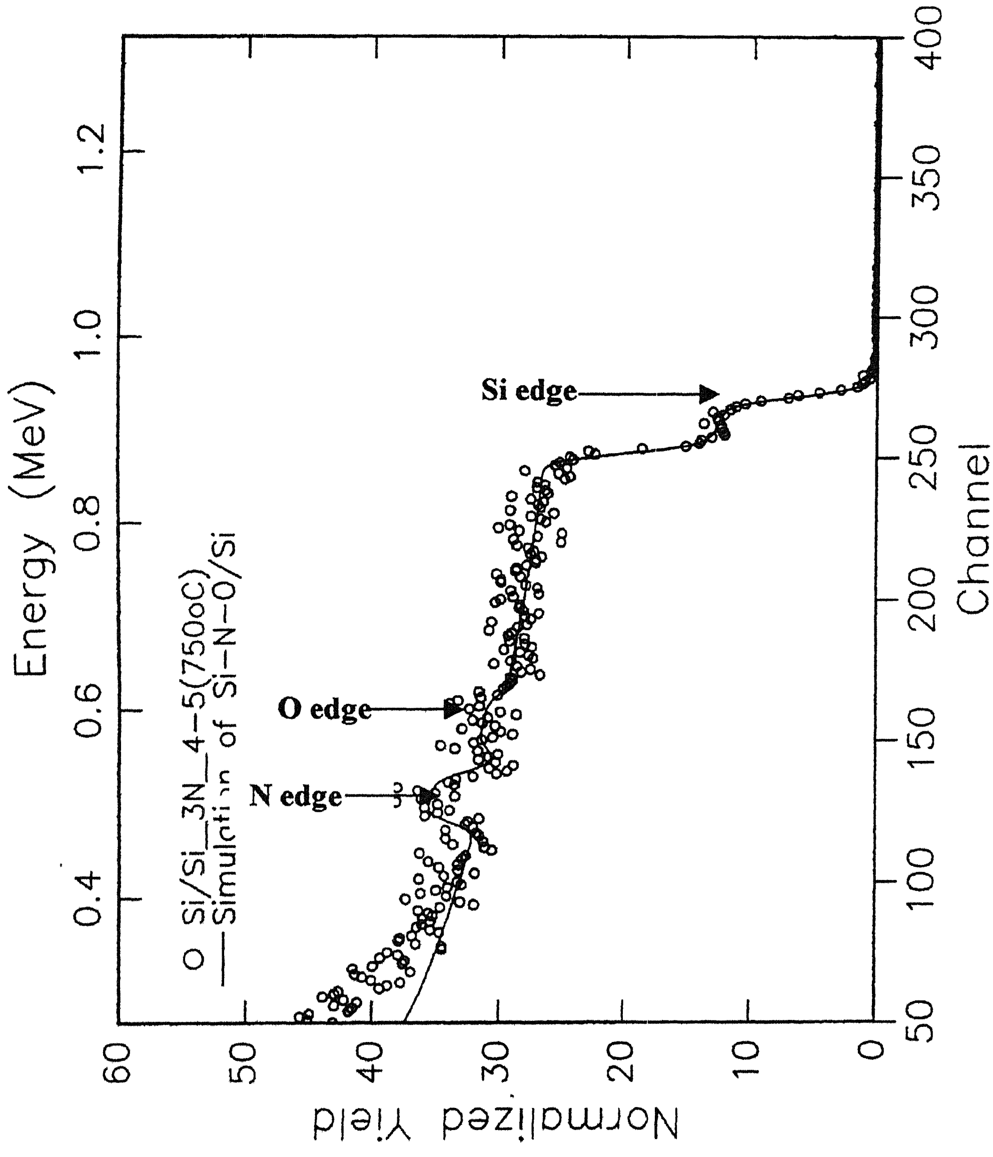


Fig. 5.2.1 RBS and simulated spectra of Silicon nitride deposited at 750 °C

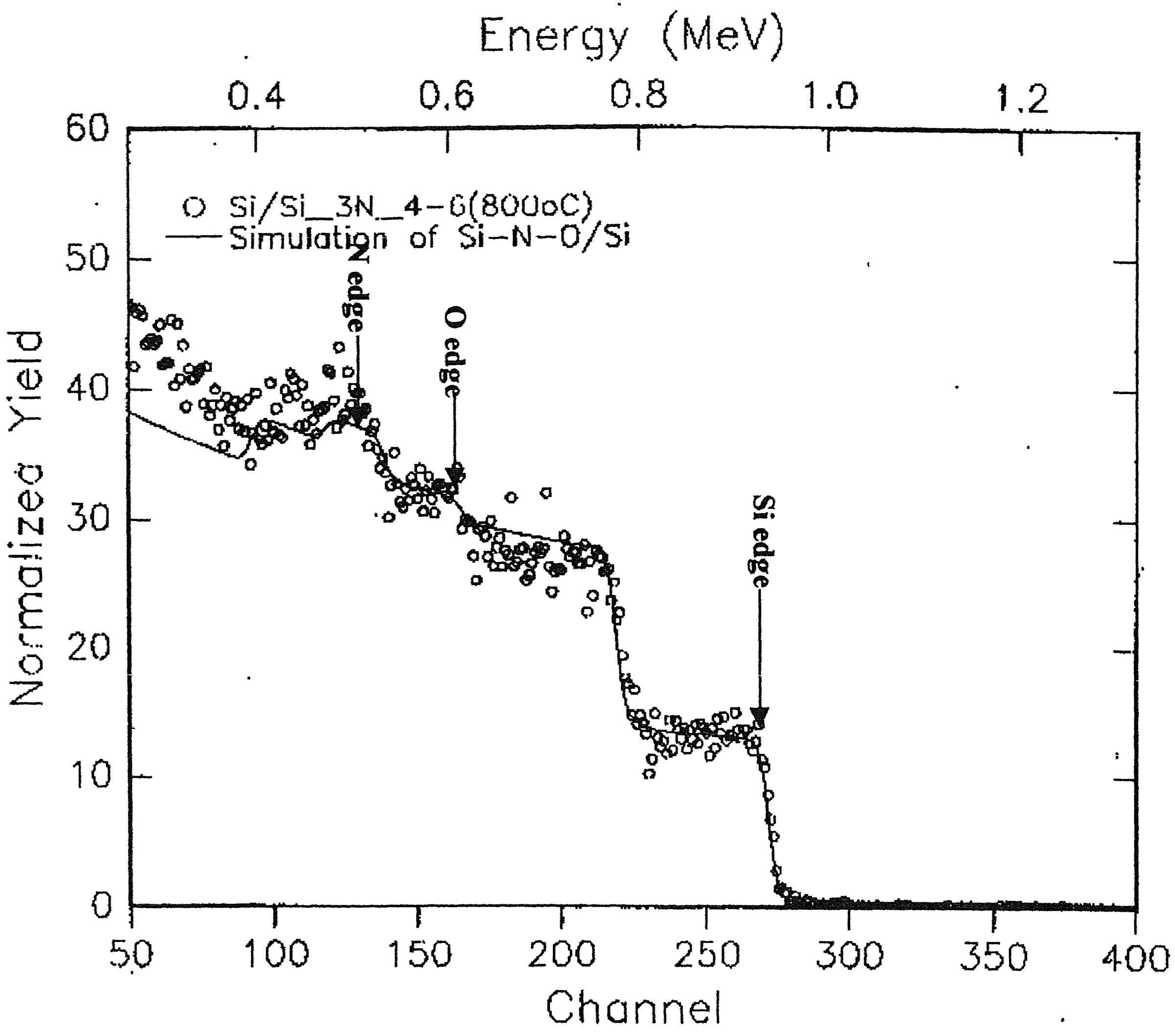


Fig. 5.2.2 RBS and simulated spectra of Silicon nitride deposited at 800 °C

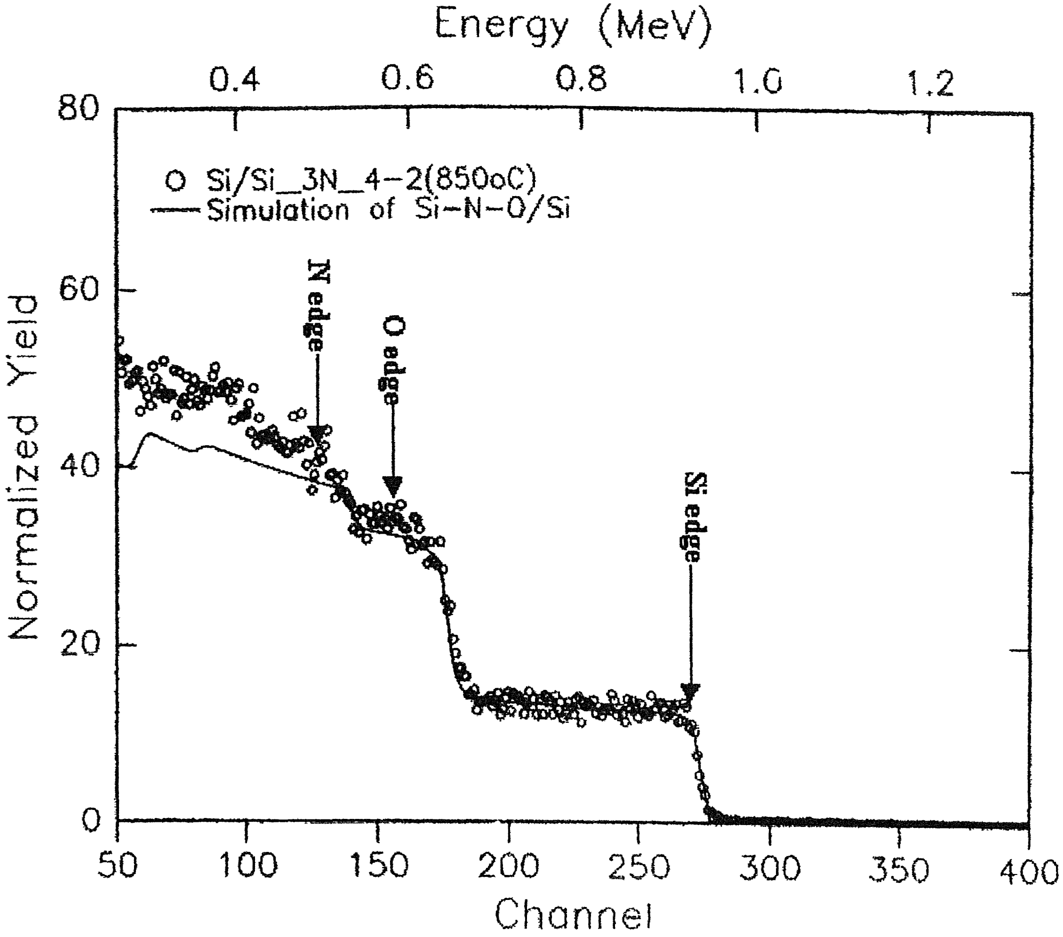
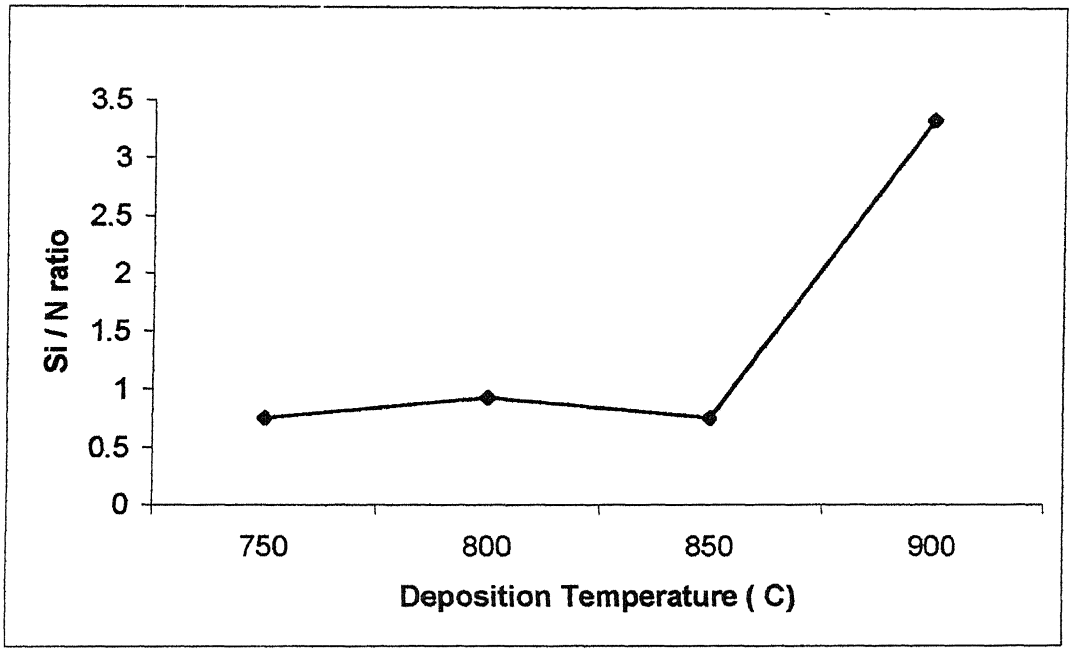
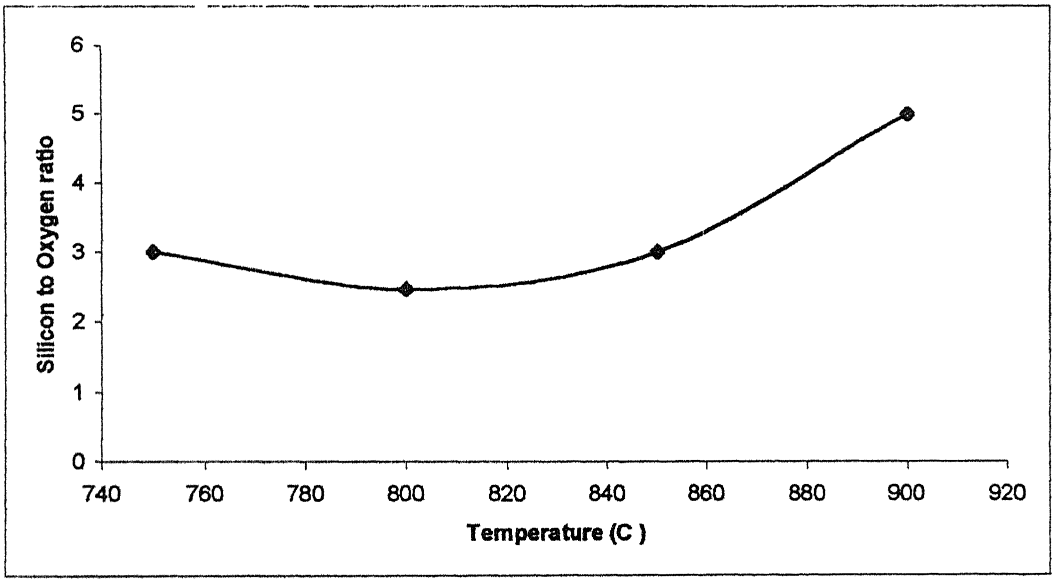


Fig. 5.2.5 RBS and simulated spectra of Silicon nitride deposited at 850°C



(a)



(b)

Fig. 5.2.6 Variation of Composition with deposition temperature (a) Silicon to Nitrogen ratio (b) Silicon to oxygen ratio.

5.3 IR Measurement

The Fourier transform infrared (FTIR) absorption spectra of silicon nitride films deposited in the temperature range of 750 to 900 °C has been taken to study the chemical nature of the films The observed spectrums were compared with the standard spectrum and were matched. They all showed a broad absorption band with maxima at 870-910 cm^{-1} depending on the deposition temperature This absorption is associated with one of the Si-N bond stretching frequencies. The observed spectrums are shown in Fig.5 3 1 to Fig. 5 3 4. The thickness of the silicon nitride films are around few thousand angstroms (1550,4000,4900,1800) and were measured by optical interference method. All the films were deposited on P-type silicon (100) wafers It is observed qualitatively that the absorption peak is shifted towards higher frequencies at higher deposition temperatures. The frequency of absorption mainly depends on mass and strength of the bond The mass of the species is not changed with change in deposition temperature, so it can be infer that, as the deposition temperature increases the strength of Si-N bond also increases In the spectrum Si-O and N-H bond absorptions peaks are also observed.

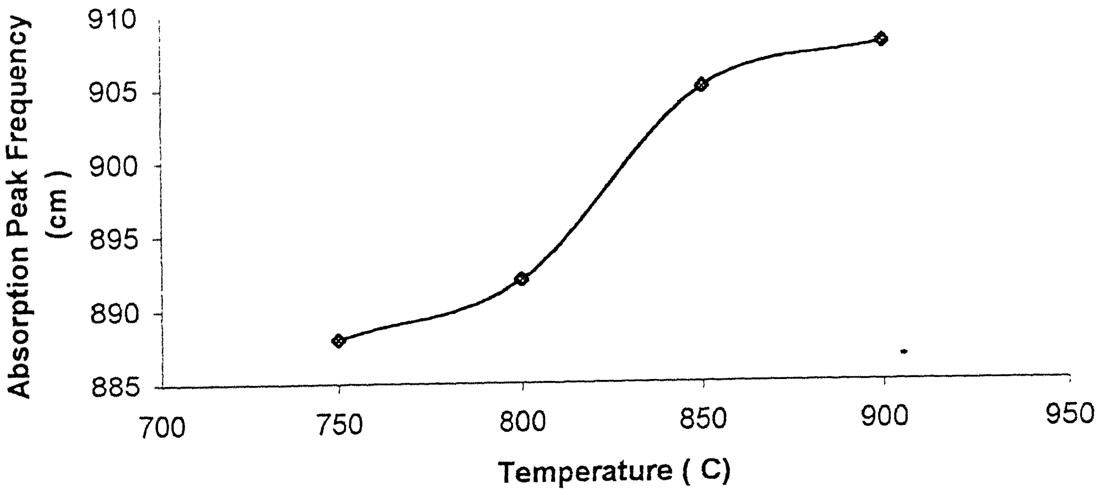


Fig. 5.3. IR Absorption Peak shift with deposition temperature

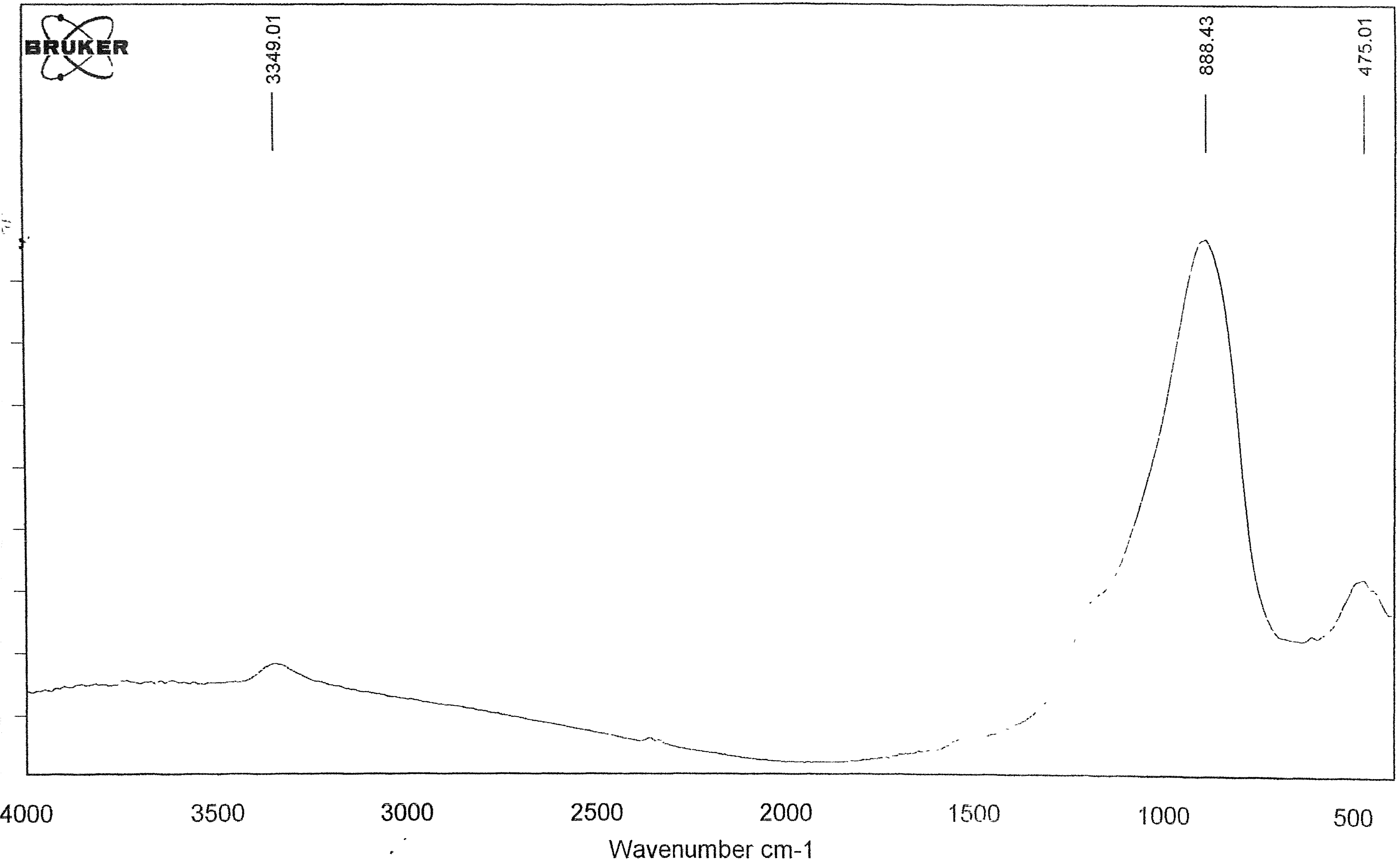


Fig.5.3.1 IR absorption spectra of silicon nitride deposited at 750°C

5.4 Interference Measurement

The refractive index of the silicon nitride films deposited at various temperatures was measured by optical interference technique. The sample preparation is described in chapter 3.4. The thickness of the films was also measured using this technique. Fig. 5.4.1 shows the variation of the refractive index with deposition temperature. As the deposition temperature increases refractive index is also increases except at 850 °C. It is because of variation of the composition with deposition temperature. The refractive index is observed high at 800 °C and 900 °C. It is because of richness of silicon in the films at these two temperatures.

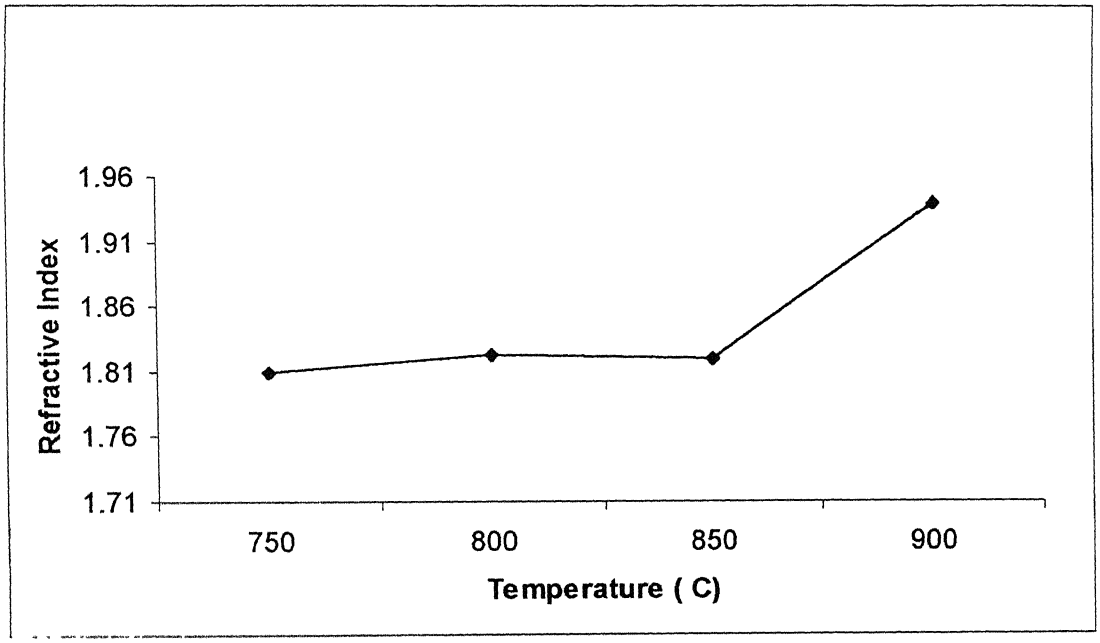


Fig. 5.4.1 Variation of Refractive Index with Deposition Temperature

5.5 CV measurement

High frequency Capacitance Voltage measurements were taken on MNS capacitors for dielectric constant measurement. Different capacitors were fabricated by depositing the silicon nitride at different temperatures. The capacitors were fabricated on n-type silicon (3.4 - 4 Ω-cm) substrates using thin films of silicon nitride. The RCA cleaning -1, RCA cleaning -2, TCA treatment of six hours at 1000 °C was done to eliminate the defects from the near surface region of the silicon wafers. Then silicon nitride was deposited at different temperatures. 2 mm diameter Aluminum metal dots were deposited by High vacuum metal evaporation unit. Measurements were done on all the capacitors fabricated by silicon nitride deposition at temperatures 750 – 900 °C. The dielectric constant was measured using eq. (3.4.1). Fig.5.5.1 shows the variation of dielectric constant with deposition temperature. As the temperature is increases the dielectric constant is also slightly increased except at 850 °C. The reason for this is richness of silicon in the films with increase of deposition temperature except at 850 °C.

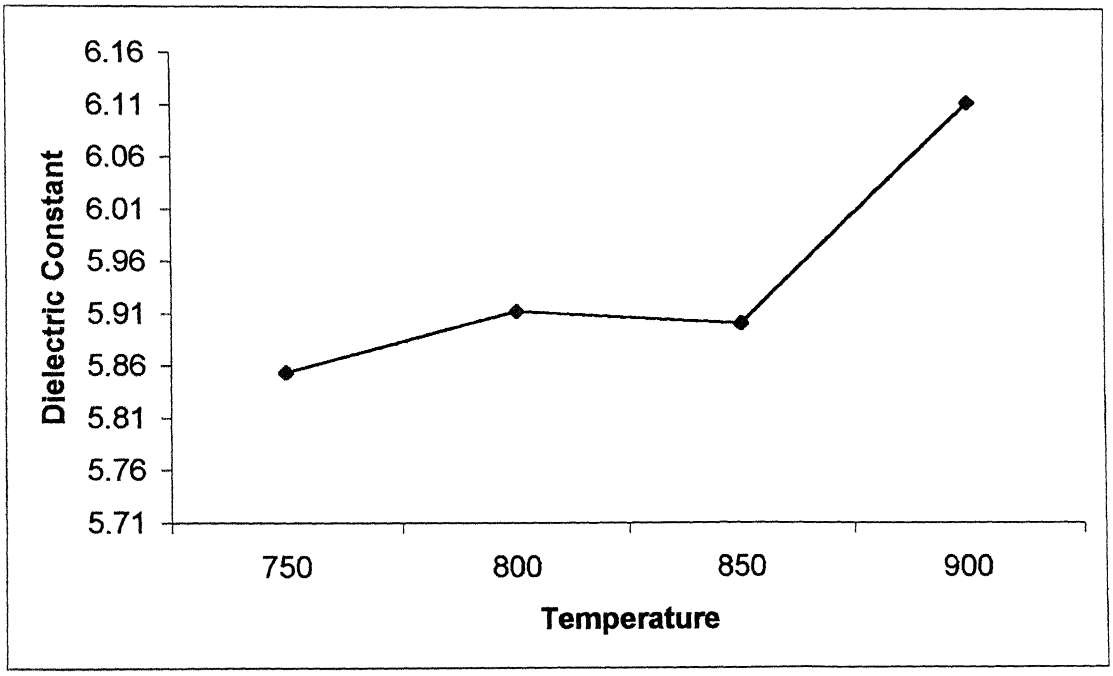


Fig. 5.5.1 Variation of Dielectric Constant with Deposition Temperature

The magnified photographs of the fabricated transistors are shown below. Fig.5.6 4 is a magnified photograph of n-channel MNOS transistor fabricated by 20 A° wet oxide and 1400 A° silicon nitride, Fig.5.6.5 is p-channel MNOS transistor fabricated by 40 A° dry oxide and 1250 A° silicon nitride, Fig. 5.6.6 is p-channel MNOS transistor fabricated by 60 A° dry oxide and 1250 A° silicon nitride and Fig.5.6.7 is n-channel MNOS transistor fabricated by 60 A° dry oxide and 1425 A° silicon nitride. Due to some problems during the fabrication of the transistors, source and drain are shorted. They are even not showing any transistor action. The problem might be diffusion failure or mask alignment failure during the fabrication process. Or the wafers might contain large amount of defect density.

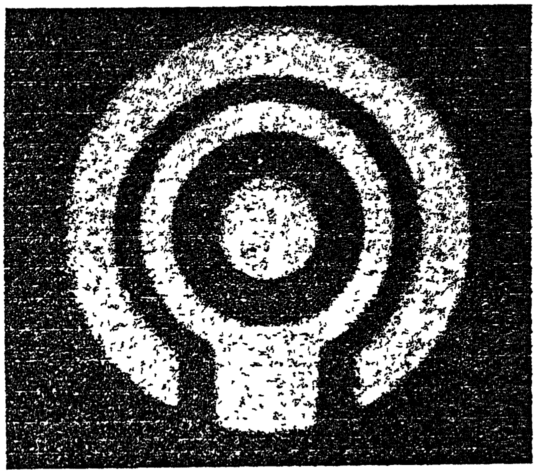


Fig.5.6.4. Magnified picture of n-channel MNOS transistor fabricated. (20 A° wet oxide, 1400 A° silicon nitride)

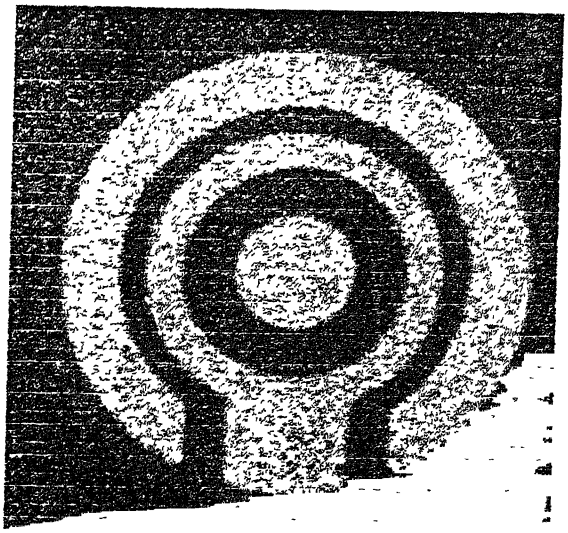


Fig.5.6.5. Magnified picture of p-channel MNOS transistor fabricated. (40 A° dry oxide, 1250 A° silicon nitride)

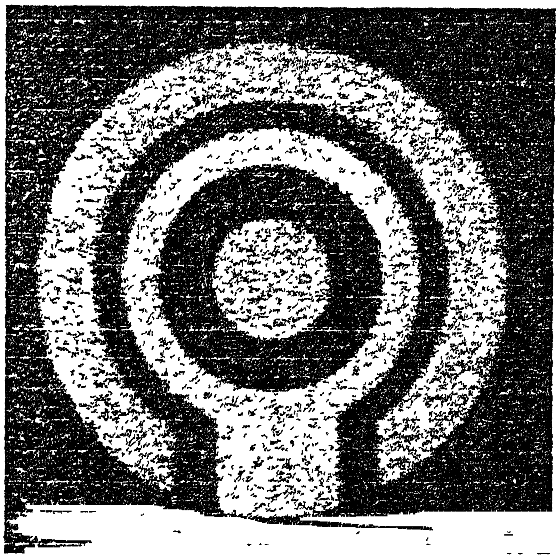


Fig.5.6.6. Magnified picture of p-channel MNOS transistor fabricated.(60-A° dry oxide, 1250 A° silicon nitride)

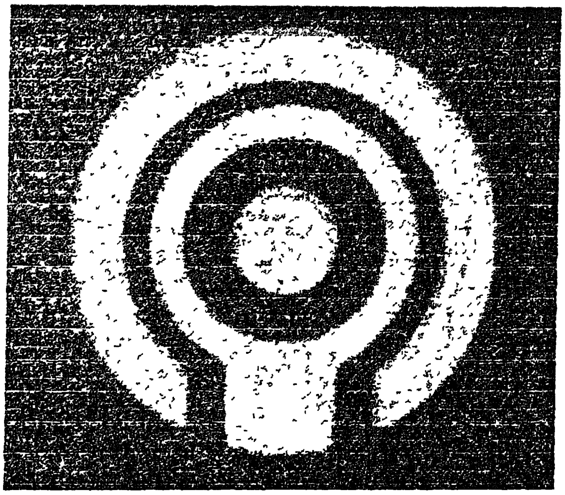


Fig.5.6.7. Magnified picture of n-channel MNOS transistor fabricated (60 A° dry oxide, 1500 A° silicon nitride)

Chapter 6

Conclusions

APCVD is a simple technique to deposit good quality, adherent and uniform CVD silicon nitride films For low ammonia to dichlorosilane ratios, uniform silicon nitride films can be deposited in the temperature range 750 –850 °C. As the temperature increase or ammonia to dichlorosilane ratio decrease the deposition rate increases Etch rate of the films decreases if the nitrogen is passed through the liquid nitrogen trap. At temperatures 750 °C, 800 °C, 850 °C, 900 °C the composition of the deposited films are Si_3N_4, $Si_{3\,7}N_4$, Si_3N_4 , $Si_5N_{1\,5}$ respectively. Silicon richness in the films increases as increase the deposition temperature except 850 °C. The strength of the Si-N bond increases as increasing the deposition temperature. Refractive index and dielectric constant increases as increasing the deposition temperature except at 850°C.

Scope for Future work

During deposition ammonium chloride was deposited in the low temperature ends of the tube and this required to clean the tube after every run. This problem can be minimized if the reactor tube is single i.e. with out brass adapter, and the reactor ends can be maintained at temperature 400 °C or by changing the reactant gas SiH_2Cl_2 by SiH_4

Since silicon nitride is not a good barrier to electrons, the tunnel charge may leaks out through the nitride. This can be minimized if another thin layer of silicon dioxide is grown on the silicon nitride i.e. MONOS devices.

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